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SPECIFICATION FOR AMOLED Module PV050FH-TONB4001

MODULE:	**PV050FH-TONB4001**
CUSTOMER:	

KINGTECH	INITIAL	DATE
PREPARED BY	Xiaoqingxia	2020.3.15
CHECKED BY	Chenzhiwen	2020.3.15
APPROVED BY	Luojiaoping	2020.3.15

CUSTOMER	INITIAL	DATE
APPROVED BY		

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REVISION STATUS

Version	Revise Date	Page	Content	Modified by
V1.0	2020.3.15	-	First Issued.	XIAO

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TABLE OF CONTENTS

1. General Description

*** Features**

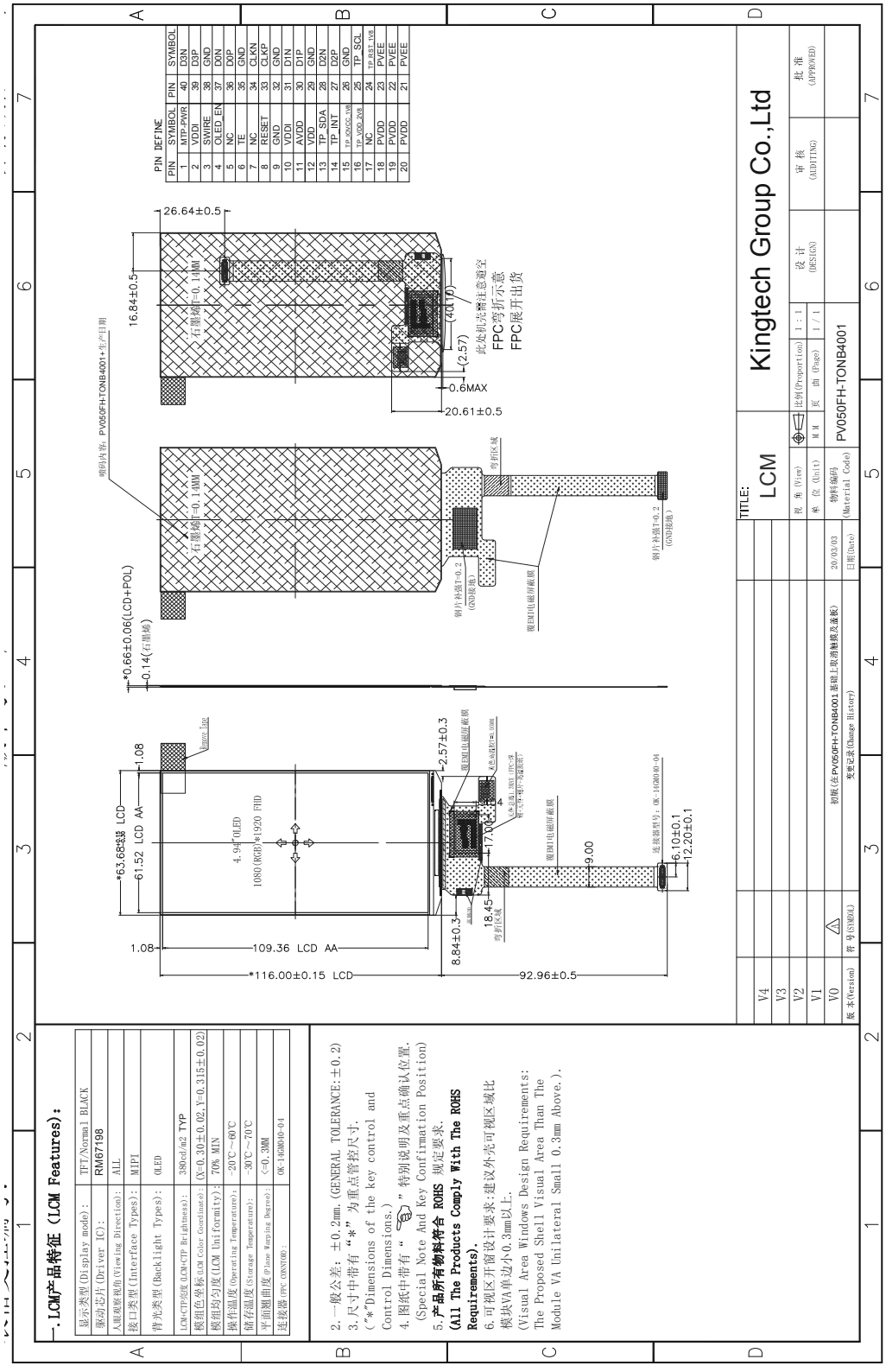
-Low Input Voltage: VDD: 2.5~3.6V;VDDI: 1.65~3.3V
-Display Colors : 16.7M colors
- Interface: MIPI-4 Lanes
-Internal Power Supply Circuit.

General Information Items	Specification	Unit	Note
	Main Panel		
Display area(AA)	61.52(H) *109.36 (V) 4.94’	mm	-
Pixel Driving element	LTPS	-	-
Display colors	16.7M	colors	-
Number of pixels	1080(RGB) *1920	dots	-
Pixel arrangement	RGB vertical stripe	-	-
Pixel pitch	0.05996 (H) *0.05996 (V)	mm	-
Viewing angle	All	o'clock	-
Drive IC	RM67198	-	-
Display mode	OLED	-	-
Operating temperature	-20～+60	℃	-
Storage temperature	-30～+70	℃	-

Mechanical Information

Item		Min.	Typ.	Max.	Unit	Note
Module size	Horizontal(H)	-	63.68	-	mm	+0.15 −0.3
	Vertical(V)	-	116.00	-	mm	±0.15
	Depth(D)	-	0.66	-	mm	±0.06
Weight		-	TBD	-	g	-

2. MECHANICAL SPECIFICATION



3. Pin Description

LCM PIN

Pin NO.	Symbol	Level	Remark
1	MTP-PWR	H/L	Signal pin
2	VDDI	H	A supply voltage
3	SWIRE	H/L	Signal pin
4	OLED_EN	H/L	Enable pin
5	NC	/	Not connect
6	TE	H/L	Tearing effect output
7	NC	/	Not connect
8	RESET	H/L	Reset signal.
9	GND	L	Ground
10	VDDI	H	A supply voltage
11	AVDD	H	A supply voltage
12	VDD	H	A supply voltage
13	TP_SDA	/	Not connect
14	TP_INT	/	Not connect
15	TP_IOVCC_1V8	/	Not connect
16	TP_VDD_2V8	/	Not connect
17	NC	/	Not connect
18	PVDD	H	A supply voltage
19	PVDD	H	A supply voltage
20	PVDD	H	A supply voltage
21	PVEE	H	A supply voltage
22	PVEE	H	A supply voltage
23	PVEE	H	A supply voltage
24	TP_RST_1V8	/	Not connect
25	TP_SCL	H/L	TP serial clock pin
26	GND	L	Ground
27	D2_P	H/L	MIPI_DP2+ are differential data signal line
28	D2_N	H/L	MIPI_DP2- are differential data signal line
29	GND	L	Ground
30	D1_P	H/L	MIPI_DP1+ are differential data signal line
31	D1_N	H/L	MIPI_DP1- are differential data signal line
32	GND	L	Ground
33	CLK_P	H/L	CLOCK Lane positive-end input pin
34	CLK_N	H/L	CLOCK Lane negative-end input pin
35	GND	L	Ground
36	D0_P	H/L	MIPI_DP0+ are differential data signal line

37	D0_N	H/L	MIPI_DP0- are differential data signal line
38	GND	L	Ground
39	D3_P	H/L	MIPI_DP3+ are differential data signal line
40	D3_N	H/L	MIPI_DP3- are differential data signal line

4. ELECTRICAL CHARACTERISTICS

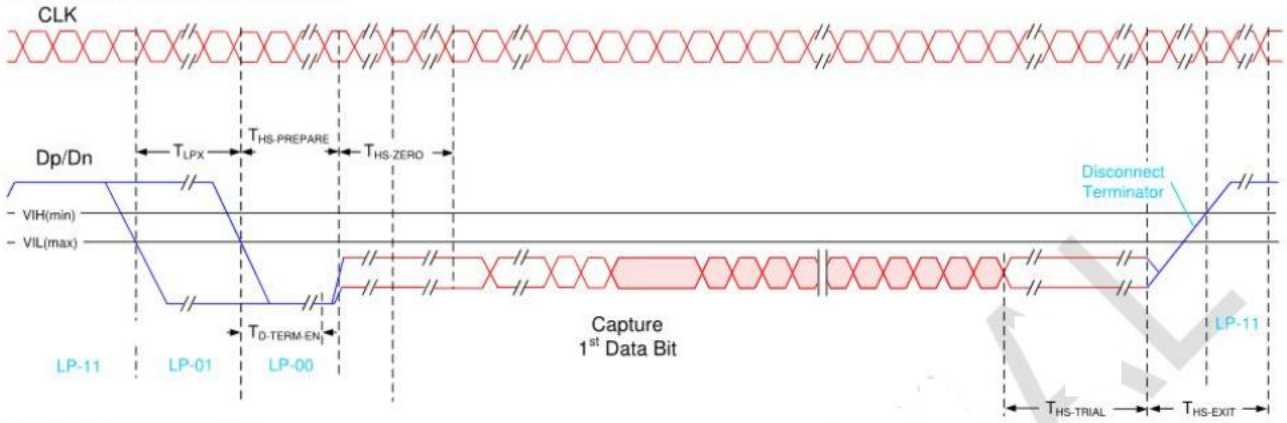
4.1 DC characteristics

Item		Symbol	Condition	Specification			Unit	Note
				Min.	Typ.	Max.		
Power & Operation Voltage								
Supply Voltage (Display)	Analog Voltage	VDD	Operation Voltage	2.5	3.3	3.6	V	
	Logic Voltage	VDDI	I/O supply voltage	1.65	1.8	3.3	V	
	Source Voltage	VLIN1		0	5.8	8	V	
	OLED positive voltage	ELVDD		4.6	4.6	5	V	
					TBD		mA	
	OLED negative voltage	ELVSS		-1.4	-2.7	-5.4	V	
					TBD		mA	
Current Consumption (Display)	Sleep out mode Display mode	I_{VDD}	Frame rate = 60HZ White pattern		TBD		mA	
		I_{VLIN1}			TBD		mA	
		I_{VDDI}			TBD		μA	
	Sleep in mode	I_{VDD}	Sleep mode		TBD		μA	
Supply Voltage (TSP)	Analog Voltage	TP_VDD		2.7	3.0	3.6	V	
	Digital Voltage	TP_IOVCC		1.71	1.8	3.6	V	
Input/ Output								
Logic Input Voltage (Display)	High Level	VIH	VDDI=1.65~3.3V	0.8VDDI	--	VDDI	V	
	Low Level	VIL		0	--	0.2VDDI		
Logic Output Voltage (Display)	High Level	VOH	IOH= -1mA IOL= +1mA	0.8VDDI	--	VDDI	V	
	Low Level	VOL		0	--	0.2VDDI		
Logic Input Current (Except MIPI/MDDI)	High level	IIHD	Vin=0~VDDI	TBD	TBD	1	μA	
	Low level	IILD	Vin=0~VDDI	-1	TBD	TBD	μA	
Logic Input Current (MIPI/ MDDI)	High level	IIHD	Vin=0~VDDAM	TBD	TBD	1	μA	
	Low level	IILD	Vin=0~VDDAM	-1	TBD	TBD	μA	
Logic Input Voltage (TSP)	Low Level	VIL		-0.3	-	0.54	V	
	High Level	VIH		1.26	-	2.1	V	

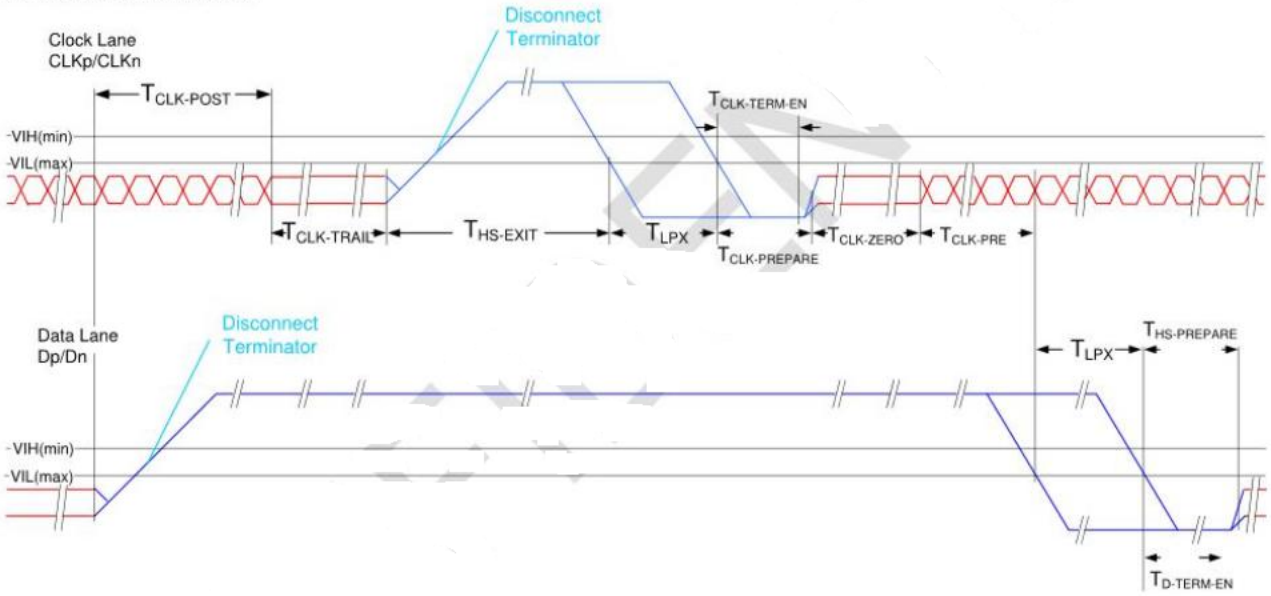
LCM+CTP Luminance	LV	–	380	-	cd/m2
Uniformity	/	70			%

4.2 MIPI Interface Characteristics

HS Data Transmission Burst

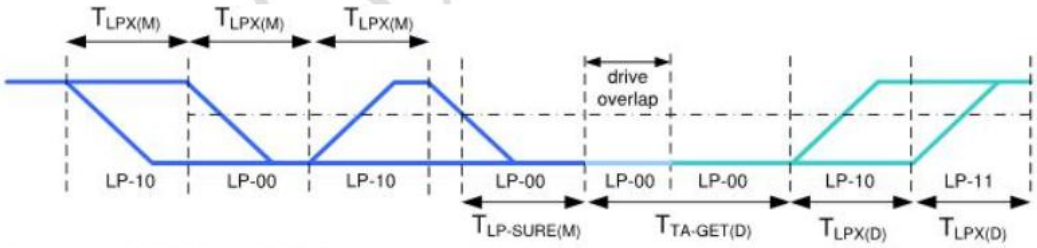


HS clock transmission

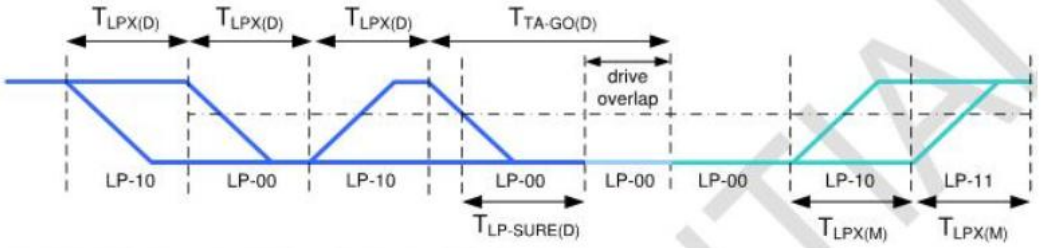


Parameter	Description	MIN	Typ	MAX	Unit
$T_{clk\text{-}post}$	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of THS-TRAIL to the beginning of TCLK-TRAIL .	60ns + 52*UI		-	ns
$T_{clk\text{-}trail}$	Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst.	60		-	ns
$T_{hs\text{-}exit}$	Time that the transmitter drives LP-11 following a HS burst.	300		-	ns
$T_{clk\text{-}term\text{-}en}$	Time for the Clock Lane receiver to	Time for Dn		38	ns

	enable the HS line termination, starting from the time point when Dn crosses $V_{IL,MAX}$.	to reach $V_{TERM-EN}$			
$T_{clk-prepage}$	Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission.	38		95	ns
$T_{clk-pre}$	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	8		-	UI
$T_{clk-prepage}$ + $T_{clk-zero}$	$T_{CLK-PREPARE}$ + time that the transmitter drives the HS-0 state prior to starting the Clock.	300			ns
$T_{d-term-en}$	Time for the Data Lane receiver to enable the HS line termination, starting from the time point when Dn crosses $V_{IL,MAX}$.	Time for Dn to reach $V_{TERM-EN}$		35 ns +4*UI	ns
$T_{hs-prepage}$	Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission.	40ns + 4*UI		85 ns + 6*UI	ns
$T_{hs-prepage}$ + $T_{hs-zero}$	$T_{HS-PREPARE}$ + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence.	145ns + 10*UI		-	ns
$T_{hs-trail}$	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst.	60ns + 4*UI		-	ns



Bus turnaround (BAT) from MPU to display module timing



Bus turnaround (BAT) from display module to MPU timing

4.3 Reset Input Timing

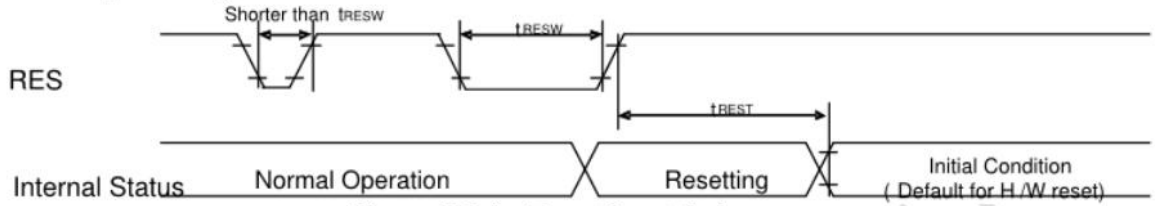


Figure 5.3.1 Reset input timing

VDDI=1.65 to 3.6V, VDD=2.5 to 3.6V, AGND=DGND=0V, Ta=-40 to 85℃

Symbol	Parameter	Related Pins	MIN	TYP	MAX	Note	Unit
t_{RESW}	*1) Reset low pulse width	RESX	10	-	-	-	us
t_{REST}	*2) Reset complete time	-	-	-	10	When reset applied during Sleep in mode	ms
		-		-	120	When reset applied during Sleep out mode	ms

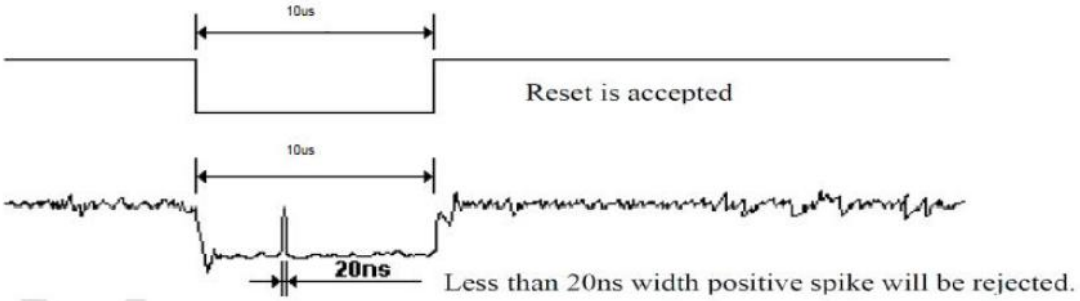
Note 1. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 30us	Reset
Between 5us and 30us	Reset starts (It depends on voltage and temperature condition.)

Note 2. During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, w en Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode) and then return to Default condition for H/W reset.

Note 3. During Reset Complete Time, data in OTP will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (tREST) within 5ms after a rising edge of RESX.

Note 4. Spike Rejection also applies during a valid reset pulse as shown below:



4. OPTICAL CHARACTERISTICS

(LCD MONOMER PARAMETERS)

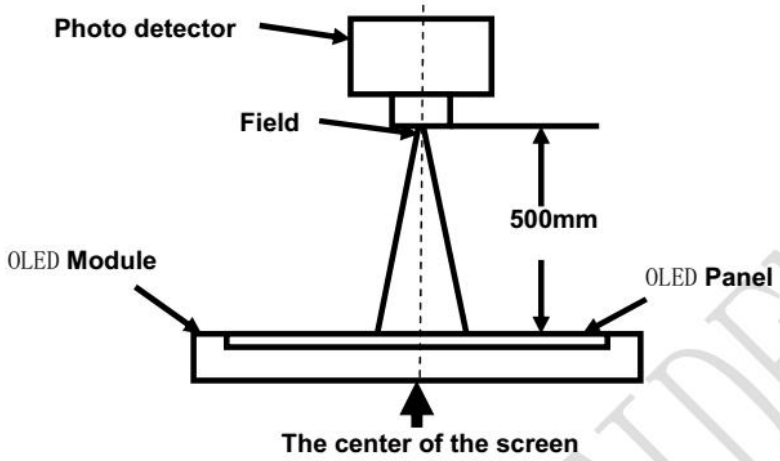
Item		Symbol	Condition	Min	Typ	Max	Unit	Remark
View Angles		θT	CR≧10	80	-	-	Degree	Note 2
		θB		80	-	-		
		θL		80	-	-		
		θR		80	-	-		
Contrast Ratio		CR	θ=0°	10000	-	-	-	Note1 Note3
Response Time		T_{ON}	25℃	-	-	1	ms	Note1 Note4
		T_{OFF}						
Chromaticity	White	x	-	0.28	0.3	0.32	-	Note5 Note1 Customer can adjust White coordinate freely
		y		0.295	0.315	0.335		
	Red	x		0.635	0.675	0.715		
		y		0.285	0.325	0.365		
	Green	x		0.175	0.235	0.295		
		y		0.657	0.717	0.777		
	Blue	x		0.096	0.136	0.176		
		y		0.012	0.052	0.092		
Uniformity		U	-	70		-	-	Note1 Note6
Color Gamut		-	-	90	104		-	Note 5
Luminance (without Lens)		L	Normal		430		-	Note1 Note7

Test Conditions:

1. The ambient temperature is 25℃.
2. The test systems refer to Note 1 and Note 2.

Note 1: Definition of optical measurement system.

The optical characteristics should be measured in dark room. After 5 minutes operation, the optical properties are measured at the center point of the OLED screen. All input terminals OLED panel must be ground when measuring the center area of the panel.



Item	Photo detector
Contrast Ratio	PR730
Luminance	
Chromaticity	
Lum Uniformity	
Response Time	DMS803

Fig. 1 Optical measurement system

Note 2: Definition of viewing angle range and measurement system.

viewing angle is measured at the center point of the OLED by PR730.

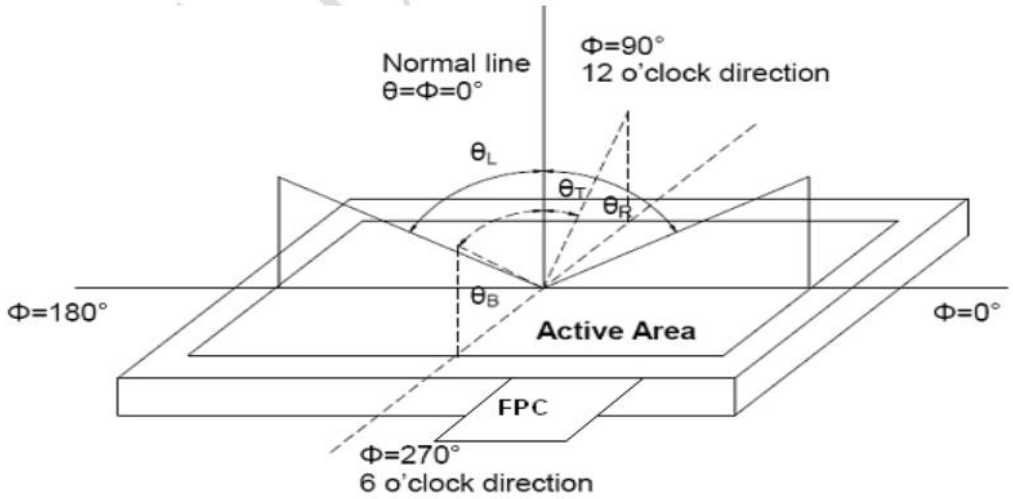


Fig. 2 Definition of viewing angle

Note 3: Definition of contrast ratio

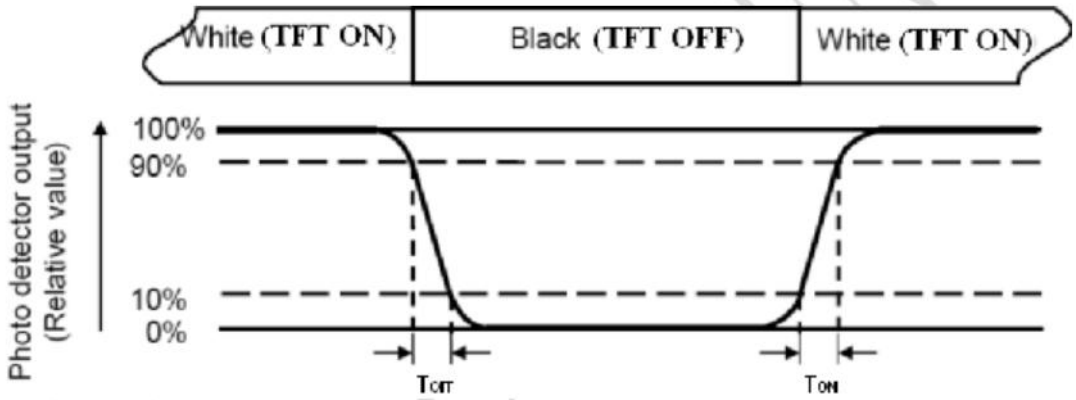
$$\text{Contrast ratio(CR)} = \frac{\text{Luminnace measured when OLED is on the "White" state}}{\text{Luminnace measured when OLED is on the "Black" state}}$$

"White state ":The state is that the OLED should be driven by Vwhite.

"Black state": The state is that the OLED should be driven by Vblack.

Note 4: Definition of Response time

The response time is defined as the OLED optical switching time interval between "White" state and "Black" state. Rise time (TON) is the time between photo detector output intensity changed from 90% to 10%. And fall time (TOFF) is the time between photo detector output intensity changed from 10% to 90%.



Note 5: Definition of color chromaticity (CIE1931)

Color coordinates measured at center point of OLED.

Note 6: Definition of Luminance Uniformity

Active area is divided into 9 measuring areas (Refer Fig. 3). Every measuring point is placed at the center of each measuring area.

Luminance Uniformity(U) = Lmin/ Lmax

L-------Active area length W----- Active area width

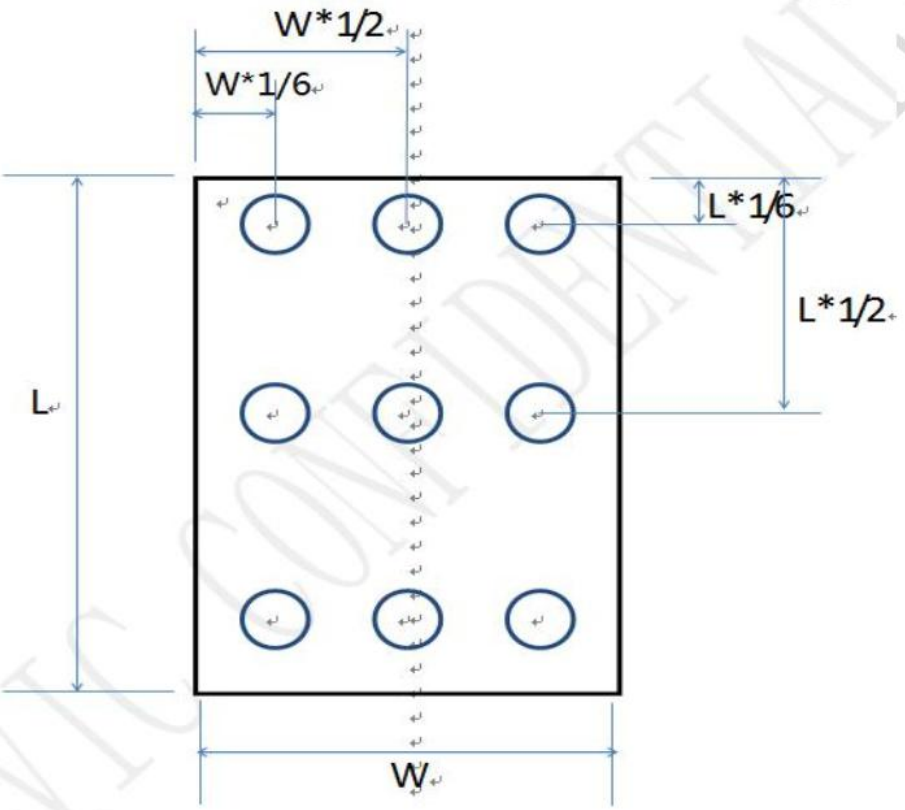


Fig. 3 Definition of uniformity

Lmax: The measured maximum luminance of all measurement position.

Lmin: The measured minimum luminance of all measurement position.

Note 7: Definition of Luminance :

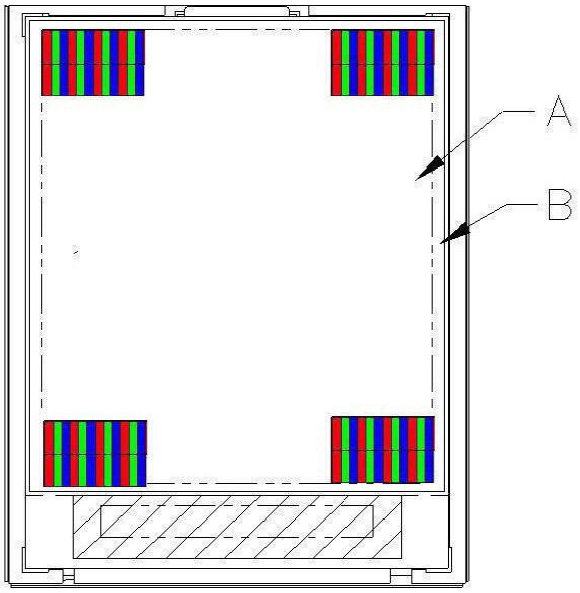
Measure the luminance of white state at center point.

6. QUALITY SPECIFICATIONS

6.1 INSPECTION CONDITION

(1) Inspect under 300~500Lux fluorescent light, leaving 30~35cm between panels and eyes, and between panels and lights.
(2) Inspection condition is 23±5°C, 50±20%RH maximum.

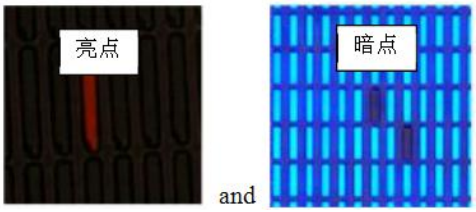
6.2 DEFINITION OF AREA



A Area : Viewing area.
B Area : Out of viewing.(outside viewing area)

6.3 INSPECTION SPECIFICATION

NO	Item	Acceptable specification	Judgment Criterion
1	Electrical Testing	**1-1 sub pixel classification** ● Sub Pixel: Number of sub pixel doesn't exceed one dot.  **Sub Pixel (Dot)** **a> Dark dot ----one Allowed** **b> Bright dot ---- one Allowed**	N≦2
		● Pixel : Three dots link together doesn't exceed ones  **Pixel**	N≦0
		1-2Leakage to light ● Leakage to light be not allowed.	N=0
		1-3Picture to shake ● Picture had shake, twinkle and noise etc. instable of defect that be not allowed.	N=0
		1-4 Function ● No display or No function. ● Source Line, Gate Line. ● Contrast Ratio ● Current consumption exceeds product specifications. ● Display malfunction.	N=0
2	Mechanical Dimension	2-1 Mechanical Dimension exceeds product specifications. 2-2 Out of frame and boss of plastic changed shape that be not allowed.	N=0

<table>
<tr><th>NO</th><th>Item</th><th>Acceptable specification</th><th>Judgment Criterion</th></tr>
<tr><td>3</td><td>Cosmetic Inspection</td><td>
3-1 Blemish: dot shapes of defect.
<table>
<tr><td>序号</td><td>检验类别</td><td>检验项目</td></tr>
<tr><td rowspan="2">3.1.1</td><td rowspan="2">点缺陷包括：像素亮/暗点/异物亮点/微小灰尘亮点等</td><td>亮点与暗点的定义：
 
</td></tr>
<tr><td>检验画面：红、绿、蓝、黑、白画
<table>
<tr><td>项目</td><td>规格</td><td></td></tr>
<tr><td rowspan="3">亮点</td><td>D≤0.1mm</td><td></td></tr>
<tr><td>0.1mm＜D≤0.2mm</td><td></td></tr>
<tr><td>D＞0.2mm</td><td></td></tr>
<tr><td rowspan="4">暗点</td><td>D≤0.1mm</td><td></td></tr>
<tr><td>0.1mm＜D≤0.2mm</td><td></td></tr>
<tr><td>0.2mm＜D≤0.3mm</td><td></td></tr>
<tr><td>D＞0.3mm</td><td></td></tr>
<tr><td>碎亮点</td><td>0.5dot< D< 1dot</td><td></td></tr>
</table></td></tr>
<tr><td>3.1.2</td><td>点混（无核）</td><td>程度≤JND2.3，N≤2，允许</td></tr>
<tr><td>3.1.3</td><td>点混（有核）</td><td>程度≤JND2.3，N≤1，核直径≤0</td></tr>
<tr><td>3.1.4</td><td>局混</td><td>程度≤JND2.2，N≤2，向内延伸 5</td></tr>
<tr><td>3.1.5</td><td>Mura</td><td>在白画面检验，使用 5%ND 滤光
OK；或双方共同订立</td></tr>
</table>
3-2 Blemish: Line shapes of defect
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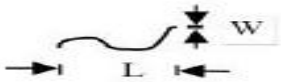
<tr><td>---</td><td>W≦0.02</td><td>Ignore</td><td rowspan="2">5 m m</td></tr>
<tr><td>L≦3.0</td><td>0.02<W≦0.05</td><td>1</td></tr>
<tr><td>L>3.0</td><td>W＞0.05</td><td>Not allowed</td><td>---</td></tr>
</table>
L: length(mm)
</td><td></td></tr>
</table>

		W: width(mm) 	
4	**Package**	4-1 Mixed product types 4-2 Shipping q'ty should be the same as "shipping notice form" q'ty. 4-3 Outer box can't broken.	N=0

7. RELIABILITY

Test Item	Test Condition
High Temperature Operation	60℃ for 96 hours
Low Temperature Operation	-20℃ for 96 hours
High Temperature Storage	70℃ for 96 hours
Low Temperature Storage	-30℃ for 96 hours
High Temperature Operation Humidity Operation	60℃, 90%RH for 72 hours
Thermal Shock	-10℃(30min) ~+25℃(5min)~ +60℃(30min) for 10 cycles
Vibration Test (No Operation)	Frequency: 10~55Hz Amplitude:1.0mm Sweep Time: 11min Test Period: 6 Cycles for each direction of X, Y, Z
Static electricity test	Touch 4KV,air touch 8KV

8. HANDLING PRECAUTION

8.1 SAFETY

(1) Do not swallow any liquid crystal, even if there is no proof that liquid stal is poisonous.
(2) If skin is exposed to liquid crystal, wash the area thoroughly with alcohol or soap.

8.2 STORAGE CONDITIONS

(1) Store the panel or module in a dark place where the temperature is 23±5℃ and thehumidity is below 50±20%RH.
(2) Store in anti-static electricity container.
(3) Store in clean environment, free from dust, active gas, and solvent.
(4) Do not place the module near organics solvents or corrosive gases.
(5) Do not crush, shake, or jolt the module.

8.3 HANDLING PRECAUTIONS

(1) Avoid static electricity which can damage the CMOS LSI.
(2) The polarizing plate of the display is very fragile. So, please handle it very carefully.
(3) Do not give external shock.
(4) Do not apply excessive force on the surface.
(5) Do not wipe the polarizing plate with a dry cloth, as it may easily scratch the surface of plate.
(6) Do not use ketonics solvent & Aromatic solvent, use with a soft cloth soaked with acleaning naphtha solvent.
(7) Do not operate it above the absolute maximum rating.
(8) Do not remove the panel or frame from the module.

8.4 WARRANTY

1) The period is within twelve months since the date of shipping out under normal using and storage conditions.
2) According to Kingtech AMOLED quality standrad,Kingtech will rework or exchange for functional defect goods sine within one year。