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SPECIFICATION FOR LCD Module PV04801TS24B

MODULE:	**PV04801TS24B**
CUSTOMER:	

KT	INITIAL	DATE
PREPARED BY	Yangrongwu	**2021.8.20**
CHECKED BY	**Chenzhiwen**	**2021.8.20**
APPROVED BY	**Luojiaoping**	**2021.8.20**

CUSTOMER	INITIAL	DATE
APPROVED BY		

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REVISION STATUS

Version	Revise Date	Page	Content	Modified by
V1.0	2021-8-20	-	First Issued.	Yang

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TABLE OF CONTENTS

1. General Description

* DESCRIPTION

PV04801TS24B is a color active matrix TFT (Thin Film Transistor) LCD (liquid crystal display) that uses amorphous silicon TFT as a switching device. This model is composed of a Transmissive type TFT-LCD Panel, driver circuit, back-light unit. The resolution of a 4.82" TFT-LCD contains 480x1120 pixels, and can display up to 16.7M colors.

* Features

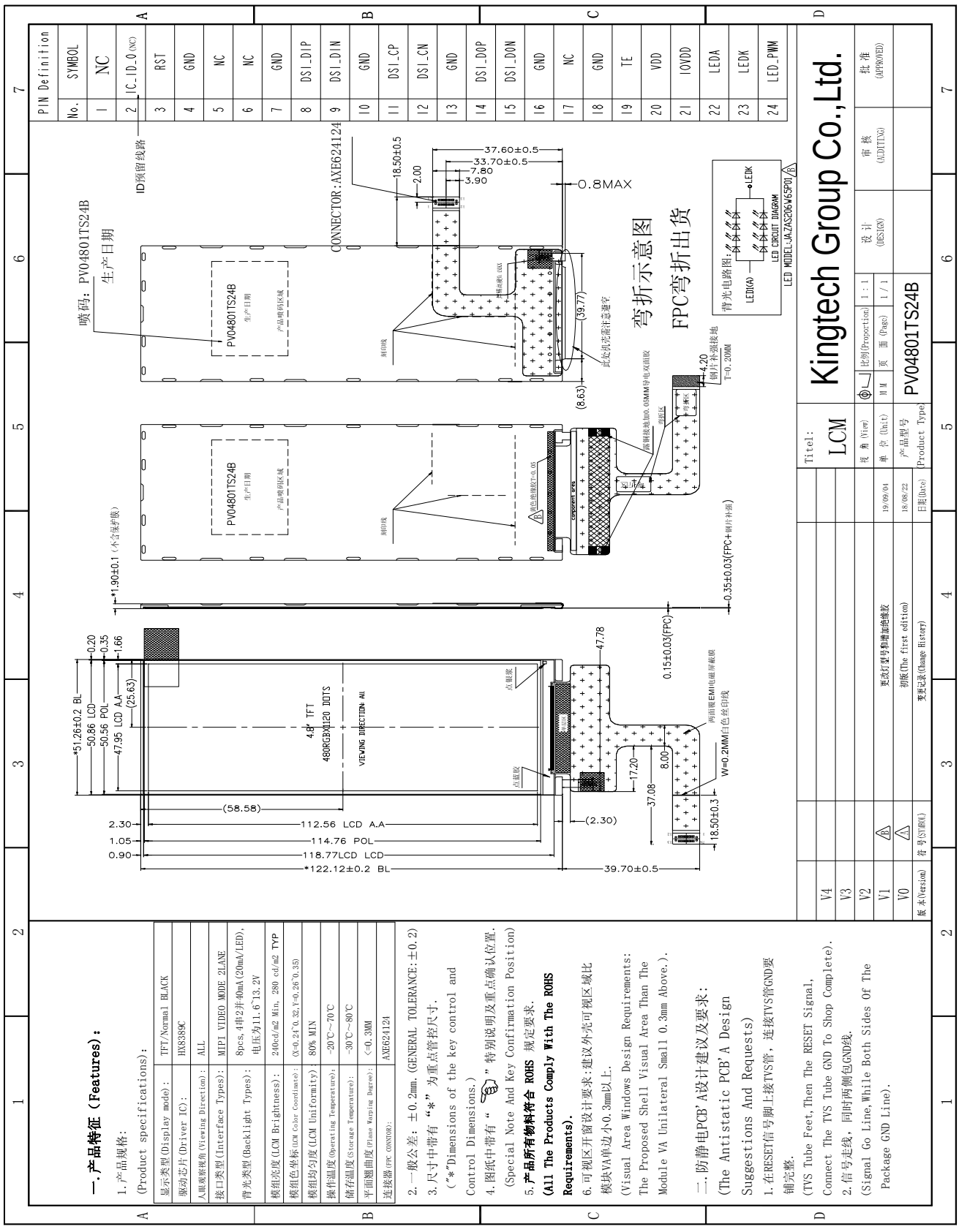
-Low Input Voltage: IOVCC: 1.65~3.3V;VCC: 2.3~3.6V
-Display Colors of TFT LCD: 16.7M colors
- Interface: MIPI VDIEO MODE 2LANE
-Internal Power Supply Circuit.

General Information Items	Specification	Unit	Note
	Main Panel		
Display area(AA)	47.95(H) *112.56 (V) (4.82 inch)	mm	-
Driver element	a-Si TFT active matrix	-	-
Display colors	16.7M	colors	-
Number of pixels	480(RGB) *1120	dots	-
Pixel arrangement	RGB vertical stripe	-	-
Pixel pitch	0.0333 (H) *0.1005 (V)	mm	-
Viewing angle	All	o'clock	-
Drive IC	HX8389C	-	-
Display mode	Normally black	-	-
Operating temperature	-20～+70	℃	-
Storage temperature	-30～+80	℃	-

Mechanical Information

Item		Min.	Typ.	Max.	Unit	Note
Module size	Horizontal(H)	-	51.26	-	mm	±0.2
	Vertical(V)	-	122.12	-	mm	±0.2
	Depth(D)	-	1.90	-	mm	±0.1
Weight		-	TBD	-	g	-

2. MECHANICAL SPECIFICATION



3. Pin Description

Pin NO.	Symbol	Level	Function
1	NC	/	Not connect
2	IC_ID_0(NC)	/	Not connect
3	RST	H/L	Hardware reset pin
4	GND	L	Ground
5	NC	/	Not connect
6	NC	/	Not connect
7	GND	L	Ground
8	DSI_DIP	H/L	Serial date input pin
9	DSI_DIN	H/L	Serial date input pin
10	GND	L	Ground
11	DSI_CP	H/L	Positive clock signal
12	DSI_CN	H/L	negative clock signal
13	GND	L	Ground
14	DSI_DOP	H/L	Serial date output pin
15	DSI-DON	H/L	Serial date output pin
16	GND	L	Ground
17	NC	/	Not connect
18	GND	L	Ground
19	TE	H/L	Tearing effect output
20	VDD	H	Power supply
21	IOVDD	H	Power supply
22	LEDA	H	Backlight+
23	LEDK	L	Backlight-
24	LED_PWM	H/L	pulsing signal

4. ELECTRICAL CHARACTERISTICS

4.1 ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Values		Unit	Remark
		Min	Max.		
Supply Voltage for Logic circuit	VDDIO	-0.3	3.6	V	
Supply Voltage for analog circuit	Vcc	-0.3	3.6	V	

4.2 DC ELECTRICAL CHARACTERISTICS

4.2.1 OPERATING CONDITIONS

Typical Operating Conditions (Ta=25℃)

Item	Symbol	Values			Unit	Remark
		Min	Typ	Max.		
Power Supply	Vcc	2.3	2.8	3.6	V	
Power Supply	VDDIO	1.65	1.8	3.3	V	
Normal mode Current consumption	Icc	-	-	65	mA	VCC=3.3V
TFT Gate ON Voltage	V_{GH}	10	-	15	V	
TFT Gate OFF Voltage	V_{GL}	-15	-	-10	V	

4.2.2 BACKLIGHT UNIT (GND=0V)

Item	Symbol	Values			Unit	Remark
		Min	Typ	Max.		
Forward supply Voltage	V_f	11.6	-	13.2	V	
Forward supply Current	I_f	-	40	-	mA	
LCM Luminance	L_V	240	280	-	cd/m2	I_B=40mA
Uniformity	/	80			%	-
Life Time			50000		Hr	

4.3

8.2 DC characteristics

(VDD2=2.5 ~3.6V, VDD3=2.5 ~ 3.6V, VDD1=1.65~3.6V, T_A=-40 ~ 85 °C)

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Input high voltage	V_{IH}	VDD1=1.65 ~ 3.6V VDD2= 2.5 ~ 3.6V VDD3= 2.5 ~ 3.6V	0.7 V_{DD1}	-	VDD1	V
Input low voltage	V_{IL}		0	-	0.3 V_{DD1}	V
OTP_PWR	V_{IH} V_{IL}	OTP_PWR	8.00V	8.25V	8.50V	V
Output high voltage (SDO, CABC_PWM_OUT, CABA_LED_EN, IDLE_ON, LED_BOOST)	V_{OH1}	I_{OH} = -1.0 mA	0.8 V_{DD1}	-	VDD1	V
Output low voltage (SDO, CABC_PWM_OUT, CABC_LED_EN, IDLE_ON, LED_BOOST)	V_{OL1}	VDD1= 1.65 ~ 3.6V I_{OL} = 1.0 mA	0	-	0.2 V_{DD1}	V
Logic High level input current	I_{IH}	VSYNC, HSYNC	-	-	1	µA
		RESX, DCX, CSX, SCL	-	-	1	µA
	I_{IHD}	DB[23:0], SDI, DCX	-	-	1	µA
		DB[23:0]	-	-	1	µA
Logic Low level input current	I_{IL}	VSYNC, HSYNC	-1	-		µA
		RESX, DCX, CSX, SCL	-1	-		µA
	I_{ILD}	DB[23:0], SDI, DCX	-1	-		µA
		DB[23:0]	-1	-		µA
Current consumption standby mode (LP-11)	$I_{ST(VDD2+VDD3)}$	VDD2/VDD3=2.8V, VDD1=1.8V HS_VCC=1.8V T_A =25°C	-	-	250	µA
Current consumption standby mode (LP-11)	$I_{ST(VDD1)}$			-	20	uA
Current consumption standby mode (LP-11)	$I_{ST(HS\_VCC)}$			-	80	uA
Current consumption standby mode (ULPS)	$I_{ST(VDD2+VDD3)}$		-	-	25	µA
Current consumption standby mode (ULPS)	$I_{ST(VDD1)}$		-	-	10	uA
Current consumption standby mode (ULPS)	$I_{ST(HS\_VCC)}$		-	-	10	uA

Note: The OTP_PWR pin is open on normal mode and in used while OTP programming condition.

8.3 AC characteristics

8.3.1 DBI Type C interface characteristics

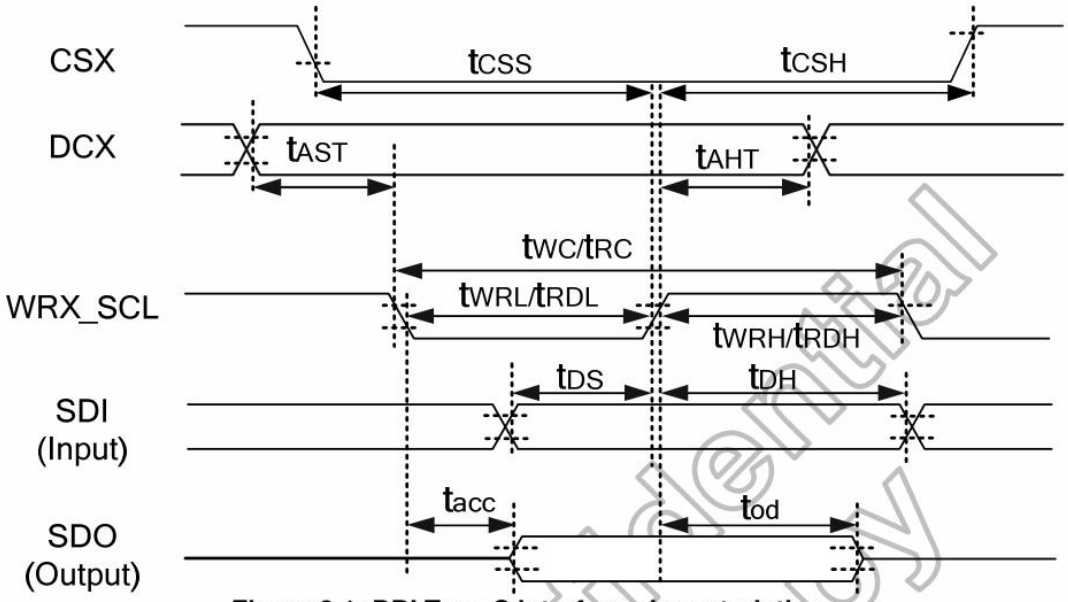


Figure 8.1: DBI Type C interface characteristics

(VSSA=0V, VDD1=1.8V, VDD2=2.8V, VDD3=2.8V, T_A = 25℃)

Signal	Symbol	Parameter	Min.	Max.	Unit	Description
CSX	t_{CSS} t_{CSH}	Chip select setup time (Write) Chip select setup time (Read)	40 40	- -	ns	-
DCX	t_{AST} I	Address setup time Address hold time (Write/Read)	10 10	- -	ns	-
WRX_SCL (Write)	t_{WC} t_{WRH} t_{WRL}	Write cycle Control pulse "H" duration Control pulse "L" duration	100 40 40	- - -	ns	-
WRX_SCL (Read)	t_{RC} t_{RDH} t_{RDL}	Read cycle Control pulse "H" duration Control pulse "L" duration	150 60 60	- - -	ns	-
SDI (Input)	t_{DS} t_{DT}	Data setup time Data hold time	30 30	- -	ns	For maximum C_L=30pF For minimum C_L=8pF
SDO (Output)	t_{RACC} t_{OD}	Read access time Output disable time	10 10	- 50	ns	

Note: The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.
Logic high and low levels are specified as 30% and 70% of VDD1 for Input signals.

Table 8.3: DBI Type C interface characteristics

8.3.2 DPI interface characteristics

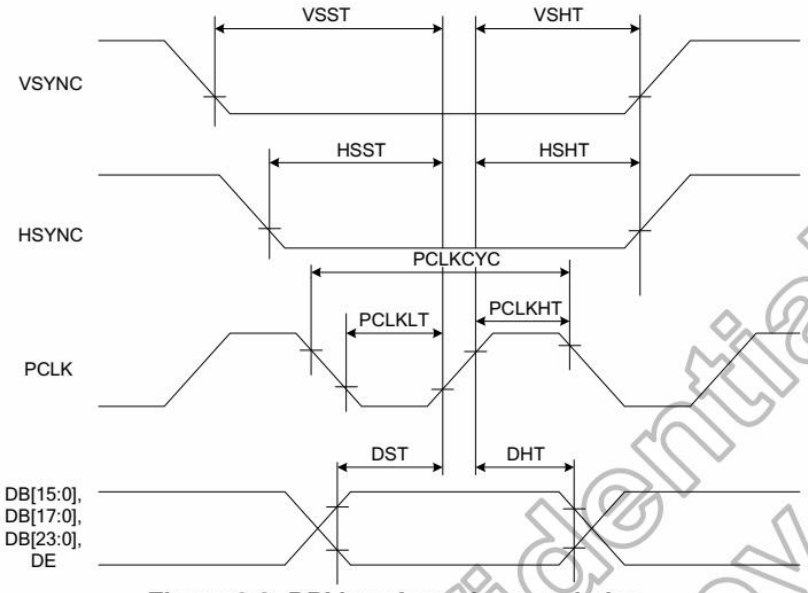


Figure 8.2: DPI interface characteristics

Resolution=540x960 (VSSA=0V, VDD1=1.8V, VDD2=2.8V, VDD3=2.8V, T_A=25℃)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Vertical sync. setup time	VSST	-	10	-	-	ns
Vertical sync. hold time	VSHT	-	10	-	-	ns
Horizontal sync. setup time	HSST	-	10	-	-	ns
Horizontal sync. hold time	HSHT	-	10	-	-	ns
Pixel clock cycle when DPI I/F is running	PCLKCYC	VRR(6) = 50 Hz	33(3)	-	36.7(4)	ns
Pixel clock low time	PCLKLT	-	10	-	-	ns
Pixel clock high time	PCLKHT	-	10	-	-	ns
Data setup time DB[23:0]	DST	-	10	-	-	ns
Data hold time DB[23:0]	DHT	-	10	-	-	ns

Resolution=540x1024 (VSSA=0V, VDD1=1.8V, VDD2=2.8V, VDD3=2.8V, T_A=25℃)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Vertical sync. setup time	VSST	-	10	-	-	ns
Vertical sync. hold time	VSHT	-	10	-	-	ns
Horizontal sync. setup time	HSST	-	10	-	-	ns
Horizontal sync. hold time	HSHT	-	10	-	-	ns
Pixel clock cycle when DPI I/F is running	PCLKCYC	VRR(6) = 46 Hz	33(3)	-	37.4(5)	ns
Pixel clock low time	PCLKLT	-	10	-	-	ns
Pixel clock high time	PCLKHT	-	10	-	-	ns
Data setup time DB[23:0]	DST	-	10	-	-	ns
Data hold time DB[23:0]	DHT	-	10	-	-	ns

Note: (1) Signal rise and fall times are equal to or less than 10 ns.
(2) Input signals are measured by 0.30 x VDD1 for low state and 0.70 x VDD1 for high state.
(3) 30 MHz
(4) 27 MHz
(5) 26.7 MHz
(6) VRR : Vertical Refresh Rate, equal to VSYNC frequency.

Table 8.4: DPI interface characteristics

Vertical Timings for DPI I/F

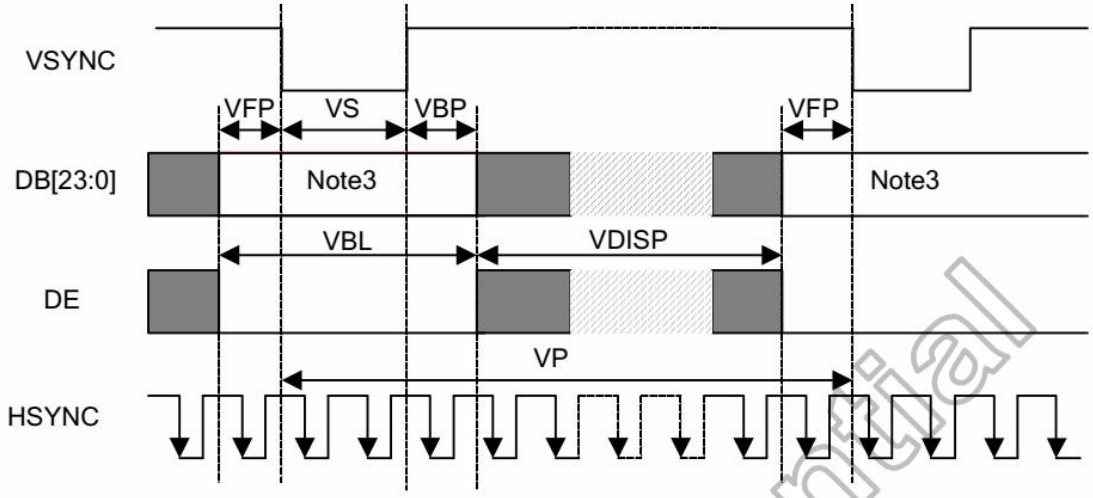


Figure 8.3: Vertical Timings for DPI I/F

Resolution=540x960(VSSA=0V, VDD1=1.8V, VDD2=2.8V, VDD3=2.8V, T_A=25℃)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Vertical cycle	VP	-	966	-	-	Line
Vertical low pulse width	VS	-	2	-	Note(4)	Line
Vertical front porch	VFP	-	2	-	-	Line
Vertical back porch	VBP	-	2	-	Note(4)	Line
Vertical data start point	-	VS+VBP	4	-	Note(4)	Line
Vertical blanking period	VBL	VS+VBP+VFP	6	-	-	Line
Vertical active area	-	VDISP	-	960	-	Line
Vertical Refresh rate	VRR	-	-	50	-	Hz

Resolution=540x1024(VSSA=0V, VDD1=1.8V, VDD2=2.8V, VDD3=2.8V, T_A=25℃)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Vertical cycle	VP	-	1030	-	-	Line
Vertical low pulse width	VS	-	2	-	Note(4)	Line
Vertical front porch	VFP	-	2	-	-	Line
Vertical back porch	VBP	-	2	-	Note(4)	Line
Vertical data start point	-	VS+VBP	4	-	Note(4)	Line
Vertical blanking period	VBL	VS+VBP+VFP	6	-	-	Line
Vertical active area	-	VDISP	-	1024	-	Line
Vertical Refresh rate	VRR	-	-	46	-	Hz

Note: (1) Signal rise and fall times are equal to or less than 10 ns.
(2) Input signals are measured by 0.30 x VDD1 for low state and 0.70 x VDD1 for highstate.
(3) Data lines can be set to "High" or "Low" during blanking time – Don't care.
(4) The VS and VBP pulse width are related to GSPand GCK timing. The GSP and GCK must be set at corresponding position for LCD normal display.

Table 8.5: Vertical Timings for DPI I/F

Horizontal Timings for DPI I/F

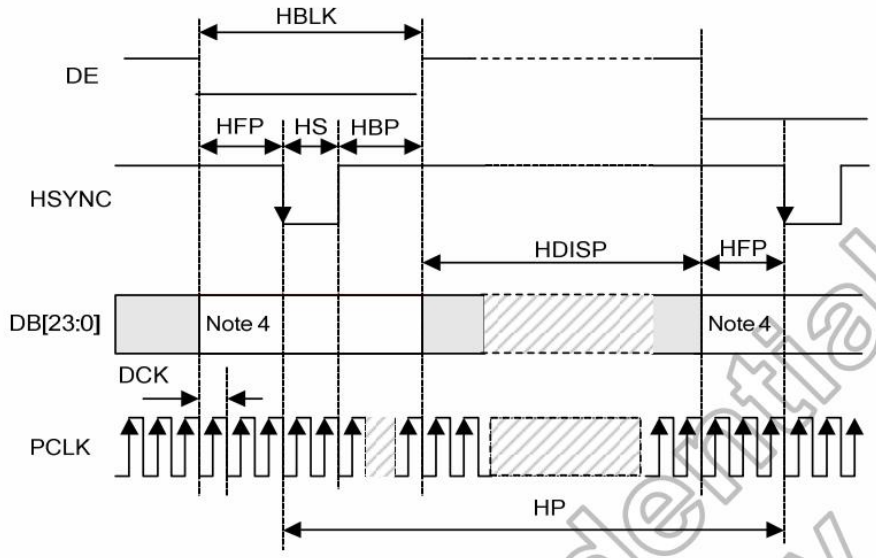


Figure 8.4: Horizontal Timing for DPI I/F

Resolution=540x960 (VSSA=0V, VDD1=1.8V, VDD2=2.8V, VDD3=2.8V, T_A=25℃)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
HS cycle	HP	Note 3	564	-	628	PCLK
HS low pulse width	HS	-	5	-	78	PCLK
Horizontal back porch	HBP	-	5	-	78	PCLK
Horizontal front porch	HFP	-	5	-	78	PCLK
Horizontal data start point	-	HS+HBP	19	-	83	PCLK
Horizontal blanking period	HBLK	HS+HBP+HFP	24	-	88	PCLK
Horizontal active area	HDISP	-	-	540	-	PCLK
Pixel clock frequency When DPI I/F is running	PCLK	VRR = 50Hz	27	-	30	MHz

Resolution=540x1024 (VSSA=0V, VDD1=1.8V, VDD2=2.8V, VDD3=2.8V, T_A=25℃)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
HS cycle	HP	Note 3	564	-	628	PCLK
HS low pulse width	HS	-	5	-	78	PCLK
Horizontal back porch	HBP	-	5	-	78	PCLK
Horizontal front porch	HFP	-	5	-	78	PCLK
Horizontal data start point	-	HS+HBP	19	-	83	PCLK
Horizontal blanking period	HBLK	HS+HBP+HFP	24	-	88	PCLK
Horizontal active area	HDISP	-	-	540	-	PCLK
Pixel clock frequency When DPI I/F is running	PCLK	VRR = 46 Hz	26.7	-	30	MHz

Note: (1) Signal rise and fall times are equal to or less than 20 ns.
(2) Input signals are measured by 0.30 x VDD1 for low state and 0.70 x VDD1 for high state.
(3) HP is multiples of eight PCLK.
(4) Data lines can be set to "High" or "Low" during blanking time – Don't care.

Table 8.6: Horizontal Timings for DPI I/F

8.3.3 Reset input timing

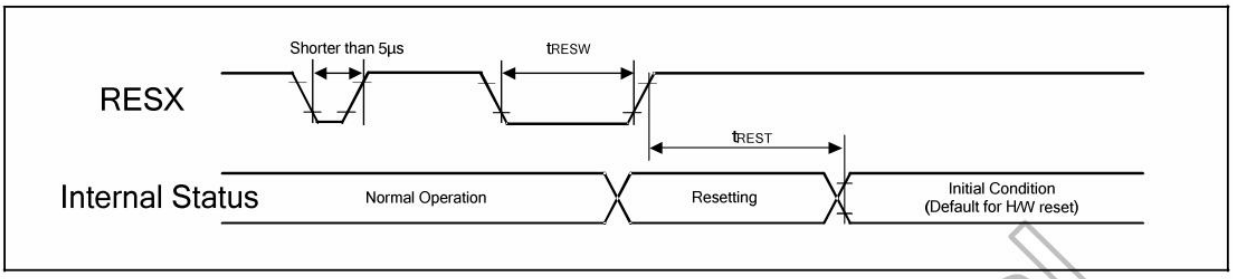


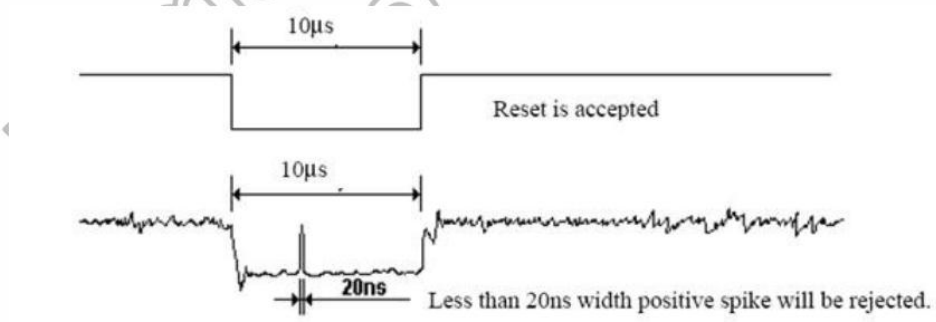
Figure 8.5: Reset input timing

Symbol	Parameter	Related pins	Min.	Typ.	Max.	Note	Unit
t_{RESW}	Reset low pulse width(1)	RESX	10	-	-	-	µs
t_{REST}	Reset complete time(2)	-	5	-	-	When reset is applied during Sleep In mode	ms
		-	120	-	-	When reset is applied during Sleep Out mode	ms

Note: (1) Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

RESX Pulse	Action
Shorter than 5 µs	Reset Rejected
Longer than 10 µs	Reset
Between 5 µs and 10 µs	Reset Start

(2) During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode) and then returns to Default condition for H/W reset.
(3) During Reset Complete Time, ID2 value in OTP will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (tREST) within 5ms after a rising edge of RESX.
(4) Spike Rejection also applies during a valid reset pulse as shown below:



(5) When Reset is applied during Sleep In Mode.
(6) When Reset is applied during Sleep Out Mode.
(7) It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

Table 8.7: Reset timing

5. OPTICAL CHARACTERISTICS

(LCM optical characteristics)

The test of Optical specifications shall be measured in a dark room(ambient luminance≤ 1 lux and temperature = 25±2℃) with the equipment of Luminance meter system (Topcon SR-UL1R and Westar TRD-100A) and test unit shall be located at an approximate distance 50cm from the LCD surface at a viewing angle of θ and Φ equal to 0°.The center of the measuring spot on the Display surface shall stay fixed.

The backlight should be operating for 30 minutes prior to measurement.

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Threshold Voltage		Vsat		4.1	4.3	4.5	V	Fig.1
		Vth		1.6	1.8	2.0	V	
Viewing Angle	Horizontal	Θ3	CR>10	70	80		°	Note 1
		Θ9		70	80		°	
	Vertical	Θ12		70	80		°	
		Θ6		70	80		°	
Contrast Ratio		CR	Θ= 0°		900			Note 2
Transmittance		T(%)	Θ= 0°		3.7			Note 3
NTSC		%	Θ= 0°		70			
Reproduction Of color	Red	Rx	Θ= 0°	0.641	0.656	0.671		Note 4 *Color filter Glass with OC
		Ry		0.312	0.327	0.342		
	Green	Gx		0.273	0.288	0.303		
		Gy		0.575	0.590	0.605		
	Blue	Bx		0.123	0.138	0.153		
		By		0.096	0.111	0.126		
White		Wx	Θ= 0°	0.287	0.302	0.317		
		Wy		0.314	0.329	0.344		
Response Time		Tr+Tf	Θ= 0°		25		ms	Note 5

Note:

1. Viewing angle is the angle at which the contrast ratio is greater than 10. The viewing are determined for the horizontal or 3, 9 o'clock direction and the vertical or 6, 12 o'clock direction with respect to the optical axis which is normal to the LCD surface (see FIG.2).
2. Contrast measurements shall be made at viewing angle of Θ= 0° and at the center of the LCD surface. Luminance shall be measured with all pixels in the view field set first to white, then to the dark (black) state. (See FIG. 2) Luminance Contrast Ratio (CR) is defined mathematically.

$$CR = \frac{\text{Luminance when displaying a white raster}}{\text{Luminance when displaying a black raster}}$$

3. Transmittance is the value with APF Pol.

4. The color chromaticity coordinates specified in Table1 shall be calculated from
The spectral data measured with all pixels first in red, green, blue and white.
Measurements shall be made at the center of the C/F.
Measurement condition is C - light source & Halogen Lamp
5. The electro-optical response time measurements shall be made as FIG.3 by switching the "data' input signal ON and OFF.
The times needed for the luminance to change from 10% to 90% is Tr, and 90% to 10% is Tf.

Figure 1. The definition of Vth & Vsat

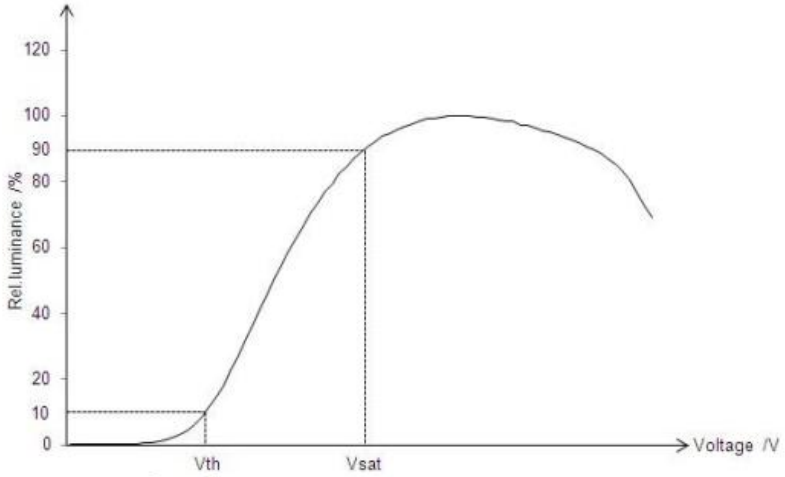


Figure 2. Measurement Set Up

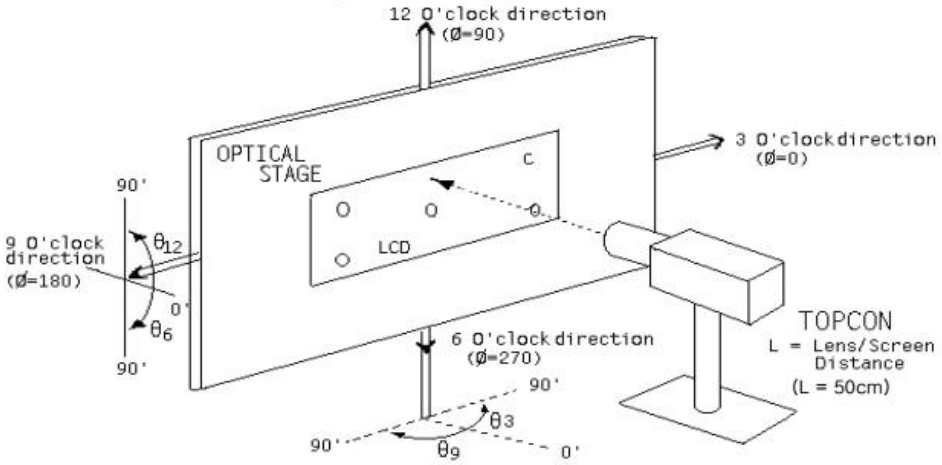
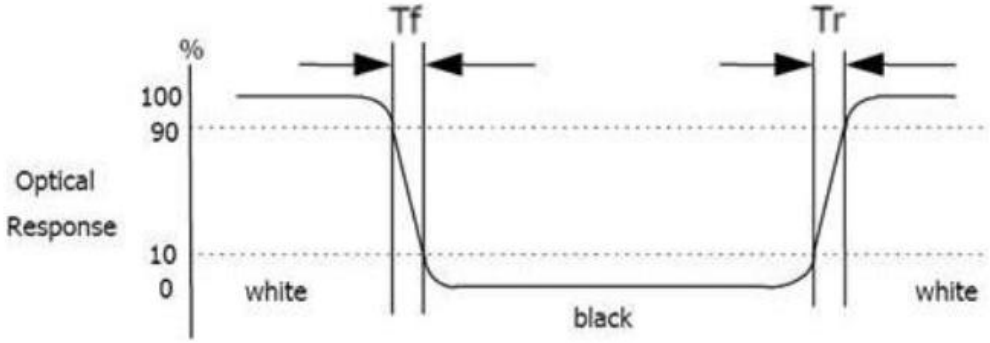


Figure 3. Response Time Testing



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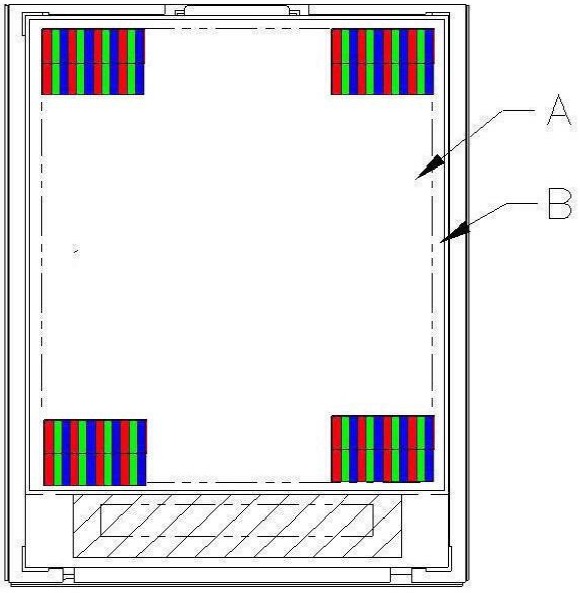
6. QUALITY SPECIFICATIONS

6.1 INSPECTION CONDITION

(1) Inspect under 300~500Lux fluorescent light, leaving 30~35cm between panels and eyes, and between panels and lights.
(2) Inspection condition is 23±5°C, 50±20%RH maximum.

6.2 DEFINITION OF AREA



A Area : Viewing area.
B Area : Out of viewing.(outside viewing area)

6.3 INSPECTION SPECIFICATION

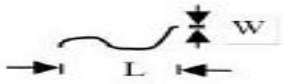
NO	Item	Acceptable specification	Judgment Criterion
1	Electrical Testing	**1-1 sub pixel classification** ● Sub Pixel: Number of sub pixel doesn't exceed one dot.  **Sub Pixel (Dot)** **a> Dark dot ----one Allowed** **b> Bright dot ---- one Allowed**	N≦2
		● Pixel : Three dots link together doesn't exceed ones  **Pixel**	N≦0
		1-2Leakage to light ● Leakage to light be not allowed.	N=0
		1-3Picture to shake ● Picture had shake, twinkle and noise etc. instable of defect that be not allowed.	N=0
		1-4 Function ● No display or No function. ● Source Line, Gate Line. ● Contrast Ratio ● Current consumption exceeds product specifications. ● Display malfunction.	N=0
2	Mechanical Dimension	2-1 Mechanical Dimension exceeds product specifications. 2-2 Out of frame and boss of plastic changed shape that be not allowed.	N=0

<table>
<tr><th>NO</th><th>Item</th><th>Acceptable specification</th><th>Judgment Criterion</th></tr>
<tr><td>3</td><td>Cosmetic Inspection</td><td>

3-1 Blemish: Line shapes of defect

<table>
<tr><th>Length</th><th>Width</th><th>Acceptable number</th><th>Mini. space</th></tr>
<tr><td>---</td><td>W≦0.05</td><td>Ignore</td><td rowspan="3">5 m m</td></tr>
<tr><td>L≦3.0</td><td>0.05<W≦0.08</td><td>4</td></tr>
<tr><td>L≦3.0</td><td>0.08<W≦0.15</td><td>3</td></tr>
<tr><td>--</td><td>W＞0.15</td><td>Not allowed</td><td>---</td></tr>
</table>

L: length(mm)
W: width(mm)



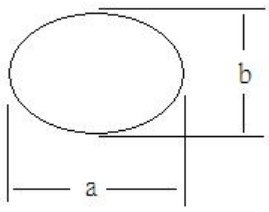
3-2 Blemish: dot shapes of defect.

<table>
<tr><th>Dimension</th><th>Acceptable number</th><th>Mini. Space</th></tr>
<tr><td>Φ≦0.15</td><td>Ignore</td><td>---</td></tr>
<tr><td>0.15＜Φ≦0.20</td><td>3</td><td rowspan="2">5 m m</td></tr>
<tr><td>0.20＜Φ≦0.30</td><td>2</td></tr>
<tr><td>Φ＞0.30</td><td>0</td><td>---</td></tr>
</table>

3-3 Polarizer Bubble

<table>
<tr><th>Dimension</th><th>Acceptable number</th><th>Mini. Space</th></tr>
<tr><td>Φ≦0.25</td><td>Ignore</td><td>---</td></tr>
<tr><td>0.25＜Φ≦0.35</td><td>3</td><td>15 m m</td></tr>
<tr><td>Φ＞0.35</td><td>0</td><td>---</td></tr>
</table>

Foreign Substances



Φ=(a+b)/2

</td><td></td></tr>
</table>

<table>
<tr><th>NO</th><th>Item</th><th>Acceptable specification</th><th>Judgment Criterion</th></tr>
<tr><td>3</td><td>Cosmetic Inspection</td><td>
3-4 Scratch
● Sensate scratch not allowed.
● Impassive scratch as below.
Unit:mm
<table>
<tr><th>Length</th><th>Width</th><th>Acceptable number</th><th>Mini. space</th></tr>
<tr><td>-----</td><td>W≦0.05</td><td>Ignore</td><td rowspan="3">5 m m</td></tr>
<tr><td>L≦3.0</td><td>0.05<W≦0.08</td><td>4</td></tr>
<tr><td>L≦3.0</td><td>0.08<W≦0.15</td><td>3</td></tr>
<tr><td>----</td><td>0.15＜W</td><td>Not allowed</td><td rowspan="2">---</td></tr>
<tr><td>L>3.0</td><td>----</td><td>Not allowed</td></tr>
</table>
</td><td></td></tr>
<tr><td>4</td><td>Package</td><td>4-1 Mixed product types
4-2 Shipping q’ty should be the same as “shipping notice form” q’ty.
4-3 Outer box can’t broken.</td><td>N=0</td></tr>
<tr><td>5</td><td>LCD Mura</td><td>LCD Mura according to ND 5% keep out to determine, if keep out distance at 30cm be seen by eyes is NG, otherwise will be ok if invisible.</td><td></td></tr>
</table>

7. RELIABILITY

Test Item	Test Condition
High Temperature Operation	70℃ for 96 hours
Low Temperature Operation	-20℃ for 96 hours
High Temperature Storage	80℃ for 96 hours
Low Temperature Storage	-30℃ for 96 hours
High Temperature Operation Humidity Operation	60℃, 90%RH for 72 hours
Thermal Shock	-10℃(30min) ~+25℃(5min)~ +60℃(30min) for 10 cycles
Vibration Test (No Operation)	Frequency: 10~55Hz Amplitude:1.0mm Sweep Time: 11min Test Period: 6 Cycles for each direction of X, Y, Z
Static electricity test	Touch 4KV,air touch 8KV

8. HANDLING PRECAUTION

8.1 SAFETY

(1) Do not swallow any liquid crystal, even if there is no proof that liquid stal is poisonous.
(2) If the LCD panel breaks, be careful not to get liquid crystal to touch your skin.
(3) If skin is exposed to liquid crystal, wash the area thoroughly with alcohol or soap.

8.2 STORAGE CONDITIONS

(1) Store the panel or module in a dark place where the temperature is 23±5℃ and thehumidity is below 50±20%RH.
(2) Store in anti-static electricity container.
(3) Store in clean environment, free from dust, active gas, and solvent.
(4) Do not place the module near organics solvents or corrosive gases.
(5) Do not crush, shake, or jolt the module.

8.3 HANDLING PRECAUTIONS

(1) Avoid static electricity which can damage the CMOS LSI.
(2) The polarizing plate of the display is very fragile. So, please handle it very carefully.
(3) Do not give external shock.
(4) Do not apply excessive force on the surface.
(5) Do not wipe the polarizing plate with a dry cloth, as it may easily scratch the surface of plate.
(6) Do not use ketonics solvent & Aromatic solvent, use with a soft cloth soaked with acleaning naphtha solvent.
(7) Do not operate it above the absolute maximum rating.
(8) Do not remove the panel or frame from the module.

8.4 WARRANTY

1) The period is within twelve months since the date of shipping out under normal using and storage conditions.
2) According to Kingtech TFT LCD quality standrad,Kingtech will rework or exchange for functional defect goods sine within one year。