



**SPECIFICATION
FOR
LCD Module
PV04302TD51D-C1**

MODULE:	PV04302TD51D-C1
CUSTOMER:	



REVISION STATUS

Version	Revise Date	Page	Content	Modified by
V1.0	2019.10.30	-	First Issued.	-



TABLE OF CONTENTS

1. General Description
2. Mechanical Characteristics
3. Pin Description
4. Electrical Characteristics
5. Optical Characteristics
6. Quality Specifications
7. Reliability
8. Handling Precaution



1. General Description

* DESCRIPTION

PV04302TD51D-C1 is a color active matrix TFT (Thin Film Transistor) LCD (liquid crystal display) that uses amorphous silicon TFT as a switching device. This model is composed of a Transmissive type TFT-LCD Panel, driver circuit, back-light unit. The resolution of a 4.3" TFT-LCD contains 480 x 800 pixels, and can display up to 16.7M colors.

* Features

- Low Input Voltage: VCC: 2.3~3.3V; IOVCC: 1.65~3.3V
- Display Colors of TFT LCD: 16.7M colors
- Interface:RGB
- Internal Power Supply Circuit.

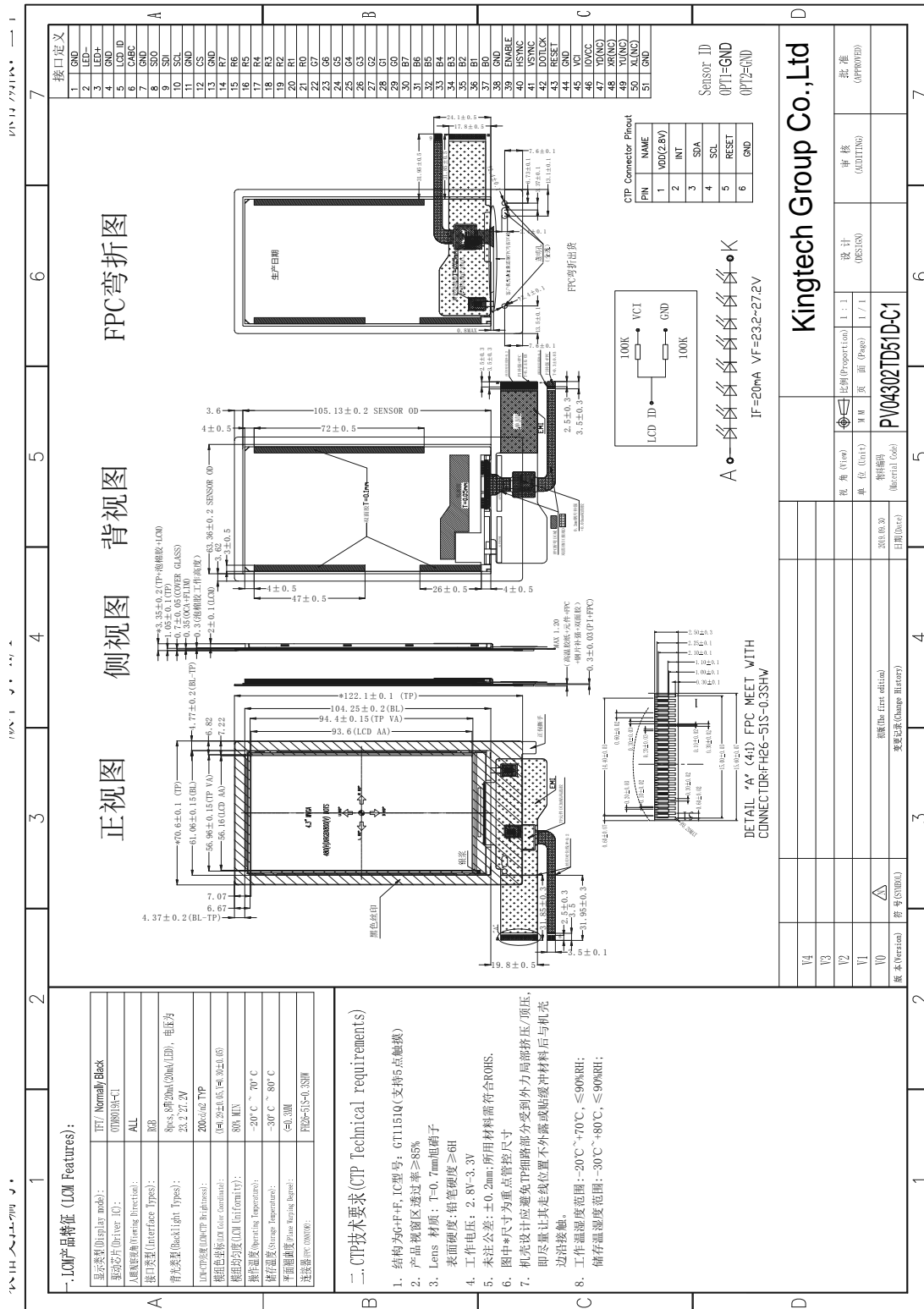
General Information Items	Specification	Unit	Note
	Main Panel		
Display area(AA)	56.16(H) *93.60(V) (4.3inch)	mm	-
Driver element	a-Si TFT active matrix	-	-
Display colors	16.7M	colors	-
Number of pixels	480(RGB) *800	dots	-
Pixel arrangement	RGB vertical stripe	-	-
Pixel pitch	0.108(H) *0.108(V)	mm	-
Viewing angle	ALL	o'clock	-
Drive IC	OTM8019A	-	-
Display mode	Normally BLACK	-	-
Operating temperature	-20~+70	°C	-
Storage temperature	-30~+80	°C	-

Mechanical Information

Item		Min.	Typ.	Max.	Unit	Note
Module size	Horizontal(H)	-	70.6	-	mm	±0.1
	Vertical(V)	-	122.1	-	mm	±0.1
	Depth(D)	-	3.35	-	mm	±0.2
Weight		-	TBD	-	g	-



2. MECHANICAL SPECIFICATION





3. Pin Description

3.1 LCM Pin Description

Pin NO.	Symbol	Level	Function
1	GND	L	Ground
2	LED-	L	Backlight-
3	LED+	H	Backlight+
4	GND	L	Ground
5	LCD_ID	H/L	Read ID
6	CABC	H/L	
7	GND	L	Ground
8	SDO	H/L	Serial data output pin
9	SDI	H/L	Serial data input pin
10	SCL	H/L	Serial communication clock input
11	GND	L	Ground
12	CS	H/L	Chip select pin
13	GND	L	Ground
14-21	R7-R0	H/L	Red data input pin
22-29	G7-G0	H/L	Green data input pin
30-37	B7-B0	H/L	Blue data input pin
38	GND	L	Ground
39	ENABLE	H/L	A data ENABLE input signal
40	HSYNC	H/L	Horizontal synchronizing signal
41	VSYNC	H/L	Vertical synchronizing signal
42	DOTCLK	H/L	Dot clock signal for RGB interface operation
43	RESET	H/L	Hardware reset pin
44	GND	L	Ground
45	VCL	H	Power supply
46	IOVCC	H	Power supply
47	YD (NC)	H/L	Not connect
48	XR (NC)	H/L	Not connect
49	YU (NC)	H/L	Not connect
50	XL (NC)	H/L	Not connect
51	GND	L	Ground



4. ELECTRICAL CHARACTERISTICS

4.1 ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Values		Unit	Remark
		Min	Max.		
Supply Voltage for Logic circuit	VDDIO	1.65	3.3	V	
Supply Voltage for analog circuit	Vcc	2.3	4.8	V	

4.2 DC ELECTRICAL CHARACTERISTICS

4.2.1 OPERATING CONDITIONS

Typical Operating Conditions (Ta=25°C)

Item	Symbol	Values			Unit	Remark
		Min	Typ	Max.		
Power Supply	Vcc	2.5	2.8	3.3	V	
Power Supply	VDDIO	1.65	1.8	3.3	V	
Normal mode Current consumption	Icc	-	80	-	mA	VCC=2.8V
TFT Gate ON Voltage	V _{GH}	12	-	18	V	
TFT Gate OFF Voltage	V _{GL}	-13.5	-	-6	V	

4.2.2 BACKLIGHT UNIT (GND=0V)

Item	Symbol	Values			Unit	Remark
		Min	Typ	Max.		
Forward supply Voltage	V _f	23.2	-	27.2	V	
Forward supply Current	I _f	-	20	-	mA	
LCM Luminance	L _v	-	200	-	cd/m ²	I _B =20mA
Uniformity	/	80			%	-



7.3.2. Reset timing characteristics

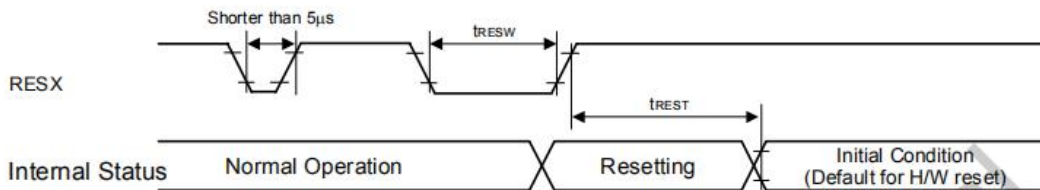


Table 7.3.2.1 Reset input timing VSS=0V, VDDIO=1.6V to 3.6V, VCI=2.5V to 5.5V, Ta = -30 to 70°C

Symbol	Parameter	Related Pins	MIN	TYP	MAX	Note	Unit
t _{RESW}	*1) Reset low pulse width	RESX	10	-	-	-	µs
t _{REST}	*2) Reset complete time	-	-	-	5	When reset applied during Sleep in mode	ms
		-	-	-	120	When reset applied during Sleep out mode	ms

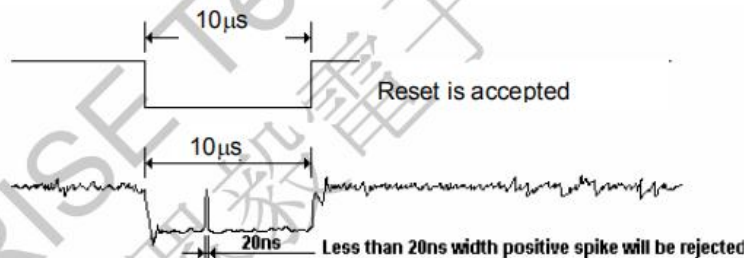
Note 1. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

RESX Pulse	Action
Shorter than 5µs	Reset Rejected
Longer than 10µs	Reset
Between 5µs and 10µs	Reset starts (It depends on voltage and temperature condition.)

Note 2. During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out-mode. The display remains the blank state in Sleep In-mode) and then return to Default condition for HW reset.

Note 3. During Reset Complete Time, ID1/ID2/ID3/ID4 and VCOM value in OTP will be latched to internal register during this period. This loading is done every time when there is HW reset complete time (t_{REST}) within 5ms after a rising edge of RESX.

Note 4. Spike Rejection also applies during a valid reset pulse as shown below:





7.3.3. Serial interface characteristics (SPI)

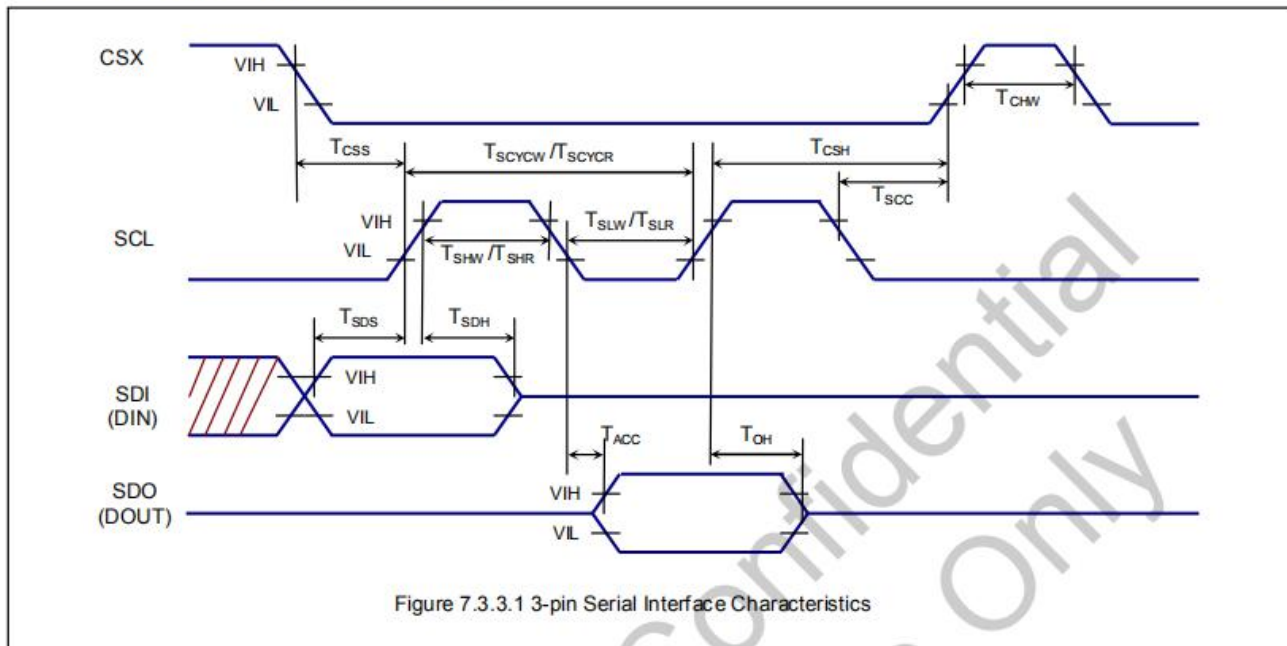


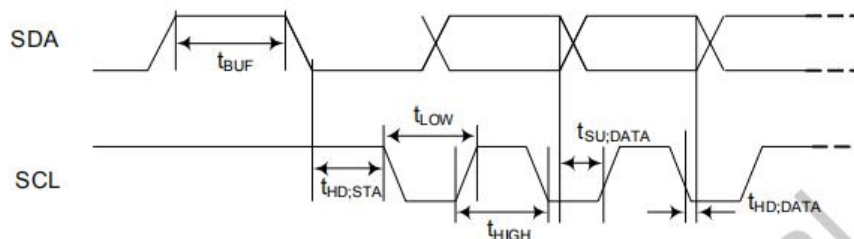
Figure 7.3.3.1 3-pin Serial Interface Characteristics

Table 7.3.3.1 SPI Interface Characteristics

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
CSX	T_{CSS}	Chip select setup time	15	-	ns	
	T_{CSH}	Chip select hold time	15	-	ns	
	T_{SCH}	Chip select setup time	20	-	ns	
	T_{CHW}	Chip select setup time	40	-	ns	
SCL	T_{SCYCW}	Serial clock cycle (Write)	66	-	ns	
	T_{SHW}	SCL "H" pulse width (Write)	10	-	ns	
	T_{SLW}	SCL "L" pulse width (Write)	10	-	ns	
	T_{SCYCR}	Serial clock cycle (Read)	150	-	ns	
	T_{SHR}	SCL "H" pulse width (Read)	60	-	ns	
SDA (DIN) (DOUT)	T_{SLR}	SCL "L" pulse width (Read)	60	-	ns	
	T_{SDS}	Data setup time	10	-	ns	
	T_{SDH}	Data hold time	10	-	ns	
	T_{ACC}	Access time	10	50	ns	For maximum $C_L=30pF$
	T_{OH}	Output disable time	15	50	ns	For minimum $C_L=8pF$

Note 1: VDDIO=1.65 to 3.6V, VDD=2.3 to 4.8V, VSSA=VSS=0V, Ta=-30 to 70°C

Note 2: The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.
Logic high and low levels are specified as 30% and 70% of VDDIO for Input signals.


7.3.4. I²C interface characteristics

 Table 7.3.4.1 I²C Interface Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f _{SCLK}	SCL clock frequency		DC	-	400	KHz
t _{LOW}	SCL clock LOW period		1.3	-	-	μs
t _{HIGH}	SCL clock HIGH period		0.6	-	-	μs
t _{SU,DATA}	data set-up time		100	-	-	ns
t _{HD,DATA}	data hold time		0	-	0.9	μs
t _R	SCL and SDA rise time	Note 2	20+0.1C _b	-	300	ns
t _F	SCL and SDA fall time	Note 2	20+0.1C _b	-	300	ns
t _F	SDA fall time for read out		20+0.1C _b	-	1000	ns
C _b	Capacitive load represented by each bus line		-	-	400	pF
t _{SU,STA}	Setup time for a repeated START condition		0.6	-	-	μs
t _{HD,STA}	START condition hold time		0.6	-	-	μs
t _{SU,STO}	Setup time for STOP condition		0.6	-	-	μs
t _{SW}	Tolerable spike width on bus	Note 1	-	-	50	ns
t _{BUF}	BUS free time between a STOP and START condition		1.3	-	-	μs

Note1: The device inputs SDA and SCL are filtered and will reject spikes on the bus lines of width $t_{SW(max)}$.

Note2: The rise and fall times specified here refer to the driver device and are part of the general fast I²C-bus specification. C_b = capacitive load per bus line.

Note3: All timing values are valid within the operating supply voltage and ambient temperature ranges and are referenced to V_{IL} and V_{OH} with an input voltage swing of VSS to VDDIO.



7.3.5. RGB interface characteristics

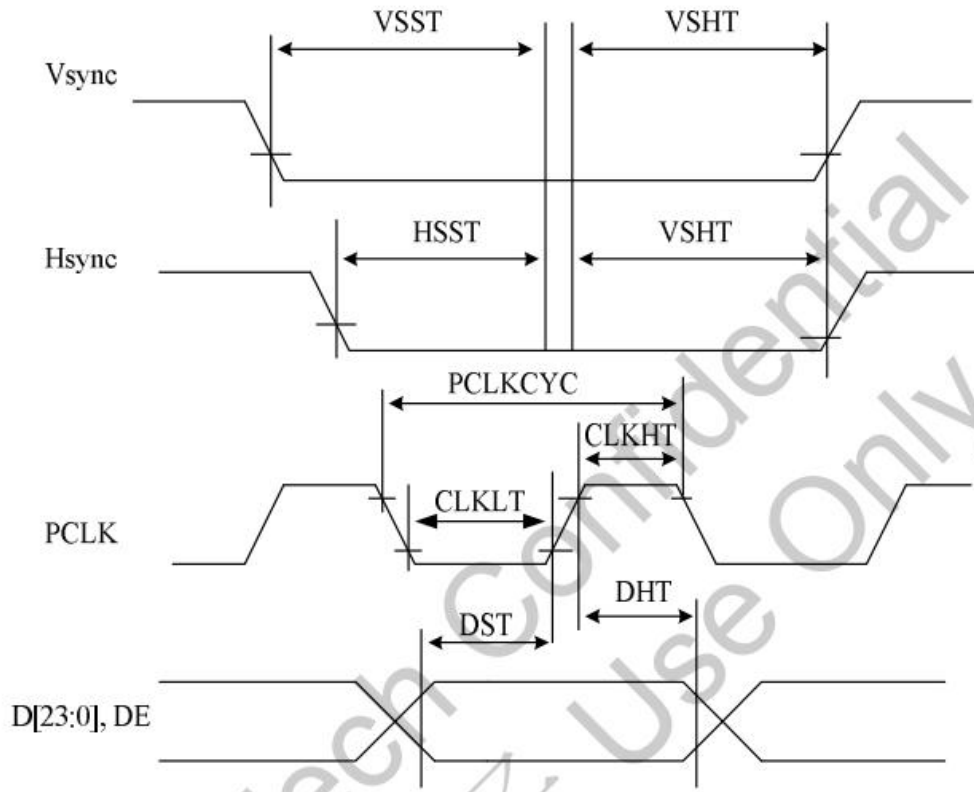


Figure 7.3.5.1 AC Timing Characteristics, RGB Interface

Table 7.3.5.1 RGB Interface Characteristics

(VDD=2.3V~4.8V, VDDIO = 1.65V~3.6V, Ta = -40°C ~ 85°C)

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
Vsync	VSST	VS setup time	5	-	ns	
	VSHT	VS hold time	5	-	ns	
Hsync	HSST	HS setup time	5	-	ns	
	HSHT	HS hold time	5	-	ns	
PCLK		Pixel clock duty cycle	33	67	%	
	PCLKLT	Pixel clock low duration	14	-	ns	
	PCLKHT	Pixel clock high duration	14	-	ns	
D [23:0], DE	DST	Data setup time	5	-	ns	
	DHT	Date hold time	5	-	ns	



5. OPTICAL CHARACTERISTICS

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Threshold Voltage		Vsat					V	Fig.1
		Vth					V	
Viewing Angle	Horizontal	Θ3	CR>10		85		Deg.	Note 1
		Θ9			85		Deg.	
	Vertical	Θ12			85		Deg.	
		Θ6			85		Deg.	
Contrast Ratio		CR	Θ= 0°	700	900			Note 2
Transmittance		T(%)	Θ= 0°		3.93%			Note 3 Base on C light W/O APF
Reproduction of color	Red	Rx	Θ= 0°	0.648	0.663	0.678		Note 4 *Color Filter Glass (with ITO) Based on C-light
		Ry		0.310	0.325	0.340		
	Green	Gx		0.256	0.271	0.386		
		Gy		0.579	0.594	0.609		
	Blue	Bx		0.119	0.134	0.149		
		By		0.107	0.122	0.137		
	White			Wx	Θ= 0°	0.277		
Wy			0.318	0.333		0.358		
Response Time		Tr+Tf	Ta= 25° C Θ= 0°		35		ms	Note 5

SPEC. NUMBER	SPEC TITLE BV040WVE-N50 –Single Cell Product Specification	PAGE 8 OF 26
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Note :

1. Viewing angle is the angle at which the contrast ratio is greater than 10. The viewing are determined for the horizontal or 3, 9 o'clock direction and the vertical or 6, 12 o'clock direction with respect to the optical axis which is normal to the LCD surface (see FIG.2).
2. Contrast measurements shall be made at viewing angle of $\theta=0^\circ$ and at the center of the LCD surface. Luminance shall be measured with all pixels in the view field set first to white, then to the dark (black) state. (See FIGURE 1 shown in Appendix) Luminance Contrast Ratio (CR) is defined mathematically.

Luminance when displaying a white raster
Luminance when displaying a black raster

- $CR = \frac{\text{Luminance when displaying a white raster}}{\text{Luminance when displaying a black raster}}$
3. Transmittance is the value with Polarizer.
 4. The color chromaticity coordinates specified in the table above shall be calculated from the spectral data measured with all pixels first in red, green, blue and white; Measurements shall be made at the center of the C/F; Measurement condition is C - light source & Halogen Lamp.
 5. The electro-optical response time measurements shall be made as FIG.3 by switching the "data" input signal ON and OFF. The times needed for the luminance to change from 10% to 90% is Tf, and 90% to 10% is Tr.



Figure 1. The definition of Vth & Vsat

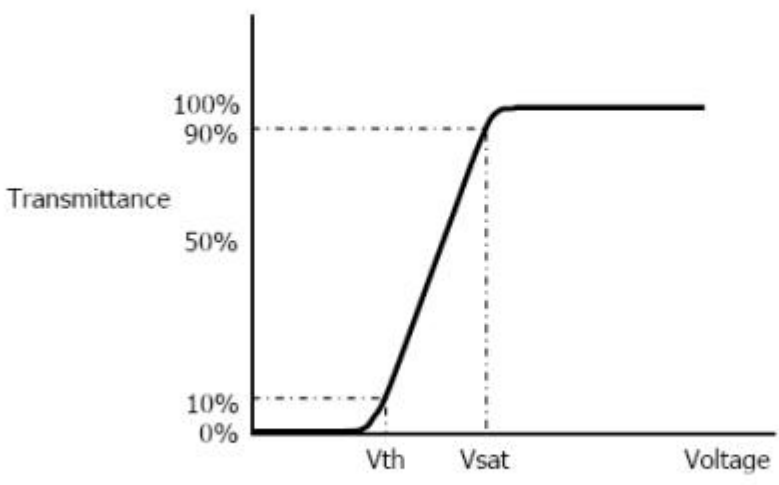




Figure 2. Measurement Set Up

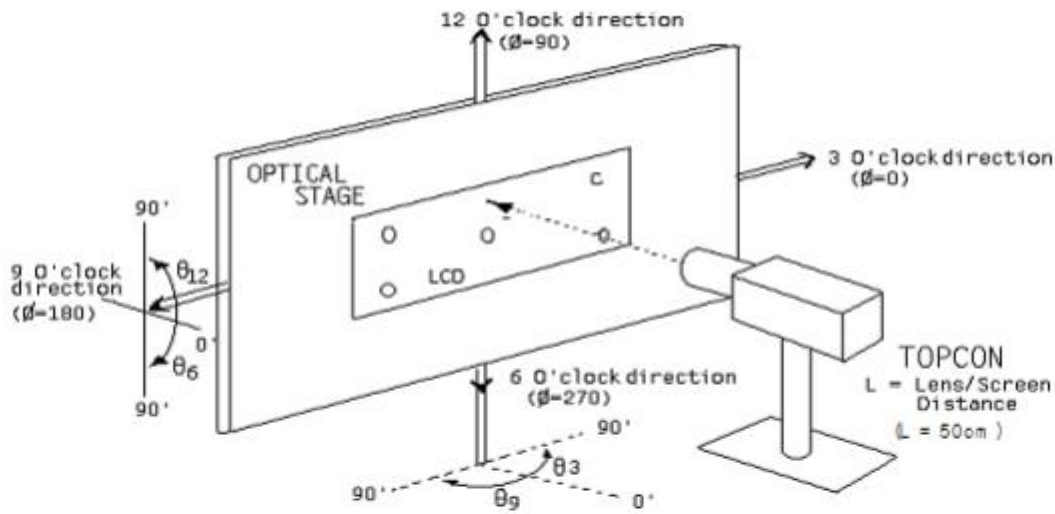
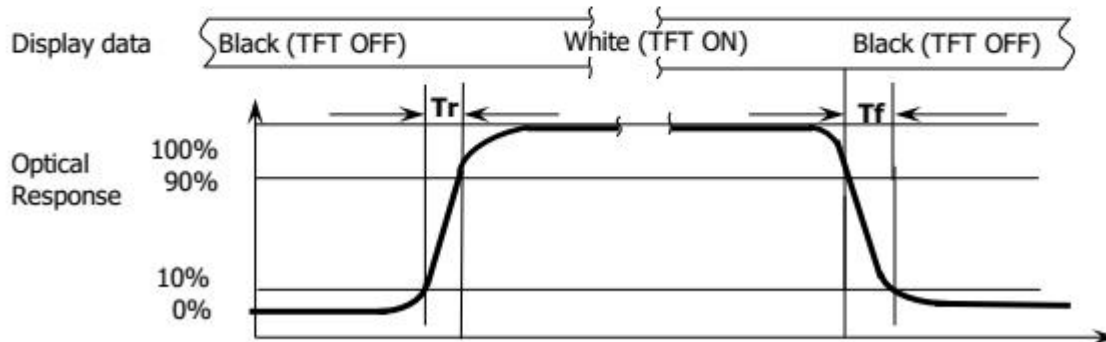


Figure 3. Response Time Testing



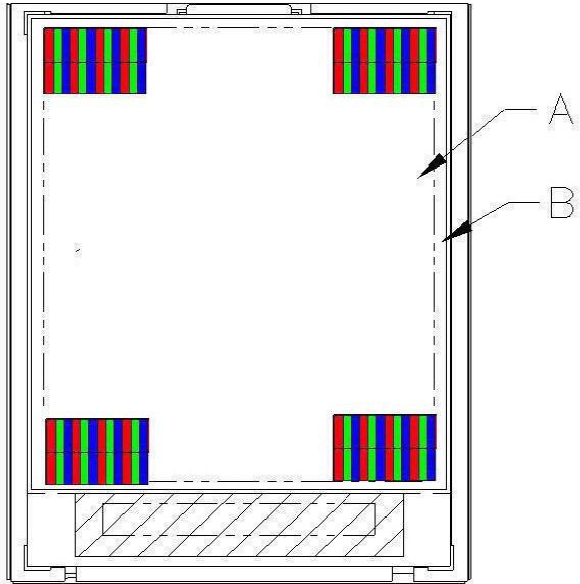
6. QUALITY SPECIFICATIONS

6.1 INSPECTION CONDITION

- (1) Inspect under 300~500Lux fluorescent light, leaving 30~35cm between panels and eyes, and between panels and lights.
- (2) Inspection condition is 23±5°C, 50±20%RH maximum.



6.2 DEFINITION OF AREA

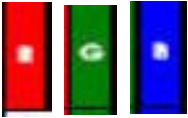



A Area : Viewing area.


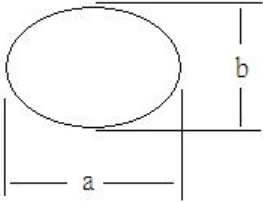
B Area : Out of viewing.(outside viewing area)



6.3 INSPECTION SPECIFICATION

NO	Item	Acceptable specification	Judgment Criterion
1	Electrical Testing	<p>1-1 sub pixel classification</p> <ul style="list-style-type: none"> Sub Pixel: Number of sub pixel doesn't exceed one dot. <div style="text-align: center;">  <p>Sub Pixel (Dot)</p> </div> <p>a> Dark dot ----one Allowed b> Bright dot ---- one Allowed</p> <ul style="list-style-type: none"> Pixel : Three dots link together doesn't exceed ones <div style="text-align: center;">  <p>Pixel</p> </div> <p>1-2 Leakage to light</p> <ul style="list-style-type: none"> Leakage to light be not allowed. <p>1-3 Picture to shake</p> <ul style="list-style-type: none"> Picture had shake, twinkle and noise etc. instable of defect that be not allowed. <p>1-4 Function</p> <ul style="list-style-type: none"> No display or No function. Source Line, Gate Line. Contrast Ratio Current consumption exceeds product specifications. Display malfunction. 	<p>$N \leq 2$</p> <p>$N \leq 0$</p> <p>$N=0$</p> <p>$N=0$</p> <p>$N=0$</p>
2	Mechanical Dimension	<p>2-1 Mechanical Dimension exceeds product specifications.</p> <p>2-2 Out of frame and boss of plastic changed shape that be not allowed.</p>	<p>$N=0$</p>



NO	Item	Acceptable specification	Judgment Criterion																																												
3	Cosmetic Inspection	<p>3-1 Blemish: Line shapes of defect</p> <table border="1" data-bbox="363 443 1315 797"> <thead> <tr> <th>Length</th> <th>Width</th> <th>Acceptable number</th> <th>Mini. space</th> </tr> </thead> <tbody> <tr> <td>---</td> <td>$W \leq 0.05$</td> <td>Ignore</td> <td rowspan="3">5 m m</td> </tr> <tr> <td>$L \leq 3.0$</td> <td>$0.05 < W \leq 0.08$</td> <td>4</td> </tr> <tr> <td>$L \leq 3.0$</td> <td>$0.08 < W \leq 0.15$</td> <td>3</td> </tr> <tr> <td>--</td> <td>$W > 0.15$</td> <td>Not allowed</td> <td>---</td> </tr> </tbody> </table> <p>L: length(mm) W: width(mm)</p>  <p>3-2 Blemish: dot shapes of defect.</p> <table border="1" data-bbox="434 1055 1283 1285"> <thead> <tr> <th>Dimension</th> <th>Acceptable number</th> <th>Mini. Space</th> </tr> </thead> <tbody> <tr> <td>$\Phi \leq 0.15$</td> <td>Ignore</td> <td>---</td> </tr> <tr> <td>$0.15 < \Phi \leq 0.20$</td> <td>3</td> <td rowspan="2">5 m m</td> </tr> <tr> <td>$0.20 < \Phi \leq 0.30$</td> <td>2</td> </tr> <tr> <td>$\Phi > 0.30$</td> <td>0</td> <td>---</td> </tr> </tbody> </table> <p>3-3 Polarizer Bubble</p> <table border="1" data-bbox="434 1361 1283 1525"> <thead> <tr> <th>Dimension</th> <th>Acceptable number</th> <th>Mini. Space</th> </tr> </thead> <tbody> <tr> <td>$\Phi \leq 0.25$</td> <td>Ignore</td> <td>---</td> </tr> <tr> <td>$0.25 < \Phi \leq 0.35$</td> <td>3</td> <td>15 m m</td> </tr> <tr> <td>$\Phi > 0.35$</td> <td>0</td> <td>---</td> </tr> </tbody> </table> <p>Foreign Substances</p>  <p>$\Phi = (a+b)/2$</p>	Length	Width	Acceptable number	Mini. space	---	$W \leq 0.05$	Ignore	5 m m	$L \leq 3.0$	$0.05 < W \leq 0.08$	4	$L \leq 3.0$	$0.08 < W \leq 0.15$	3	--	$W > 0.15$	Not allowed	---	Dimension	Acceptable number	Mini. Space	$\Phi \leq 0.15$	Ignore	---	$0.15 < \Phi \leq 0.20$	3	5 m m	$0.20 < \Phi \leq 0.30$	2	$\Phi > 0.30$	0	---	Dimension	Acceptable number	Mini. Space	$\Phi \leq 0.25$	Ignore	---	$0.25 < \Phi \leq 0.35$	3	15 m m	$\Phi > 0.35$	0	---	
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NO	Item	Acceptable specification	Judgment Criterion																					
3	Cosmetic Inspection	3-4 Scratch <ul style="list-style-type: none"> ● Sensate scratch not allowed. ● Impassive scratch as below. 																						
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		Length		Width	Acceptable number	Mini. space																		
		-----		$W \leq 0.05$	Ignore	5 m m																		
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		----		$0.15 < W$	Not allowed	---																		
		$L > 3.0$		----	Not allowed																			
4	Package	4-1 Mixed product types 4-2 Shipping q'ty should be the same as "shipping notice form" q'ty. 4-3 Outer box can't broken.	N=0																					
5	LCD Mura	LCD Mura according to ND 5% keep out to determine, if keep out distance at 30cm be seen by eyes is NG, otherwise will be ok if invisible.																						



7. RELIABILITY

Test Item	Test Condition
High Temperature Operation	70°C for 96 hours
Low Temperature Operation	-20°C for 96 hours
High Temperature Storage	80°C for 96 hours
Low Temperature Storage	-30°C for 96 hours
High Temperature Operation Humidity Operation	60°C, 90%RH for 72 hours
Thermal Shock	-10°C (30min) ~+25°C (5min)~ +60°C (30min) for 10 cycles
Vibration Test (No Operation)	Frequency: 10~55Hz Amplitude:1.0mm Sweep Time: 11min Test Period: 6 Cycles for each direction of X, Y, Z
Static electricity test	Touch 4KV,air touch 8KV



8. HANDLING PRECAUTION

8.1 SAFETY

- (1) Do not swallow any liquid crystal, even if there is no proof that liquid crystal is poisonous.
- (2) If the LCD panel breaks, be careful not to get liquid crystal to touch your skin.
- (3) If skin is exposed to liquid crystal, wash the area thoroughly with alcohol or soap.

8.2 STORAGE CONDITIONS

- (1) Store the panel or module in a dark place where the temperature is $23\pm 5^{\circ}\text{C}$ and the humidity is below $50\pm 20\% \text{RH}$.
- (2) Store in anti-static electricity container.
- (3) Store in clean environment, free from dust, active gas, and solvent.
- (4) Do not place the module near organics solvents or corrosive gases.
- (5) Do not crush, shake, or jolt the module.

8.3 HANDLING PRECAUTIONS

- (1) Avoid static electricity which can damage the CMOS LSI.
- (2) The polarizing plate of the display is very fragile. So, please handle it very carefully.
- (3) Do not give external shock.
- (4) Do not apply excessive force on the surface.
- (5) Do not wipe the polarizing plate with a dry cloth, as it may easily scratch the surface of plate.
- (6) Do not use ketonic solvent & Aromatic solvent, use with a soft cloth soaked with a cleaning naphtha solvent.
- (7) Do not operate it above the absolute maximum rating.
- (8) Do not remove the panel or frame from the module.

8.4 WARRANTY

- 1) The period is within twelve months since the date of shipping out under normal using and storage conditions.
- 2) According to KINGTECH TFT LCD quality standard KINGTECH will rework or exchange for functional defect goods since within one year.