LCM FULL SPEC

PRODUCT NO. : PV143000F0124

CUSTOMER NO. :

CUSTOMER P/N :

DRAWING VERSION : A

SAMPLE NO. :

SPEC VERSION : V1.0

CUSTOMER APPROVED	

☐Preliminary specification
■ Formal specification

APPROVED BY	CHECKED BY	PRERARED BY

CONTENT

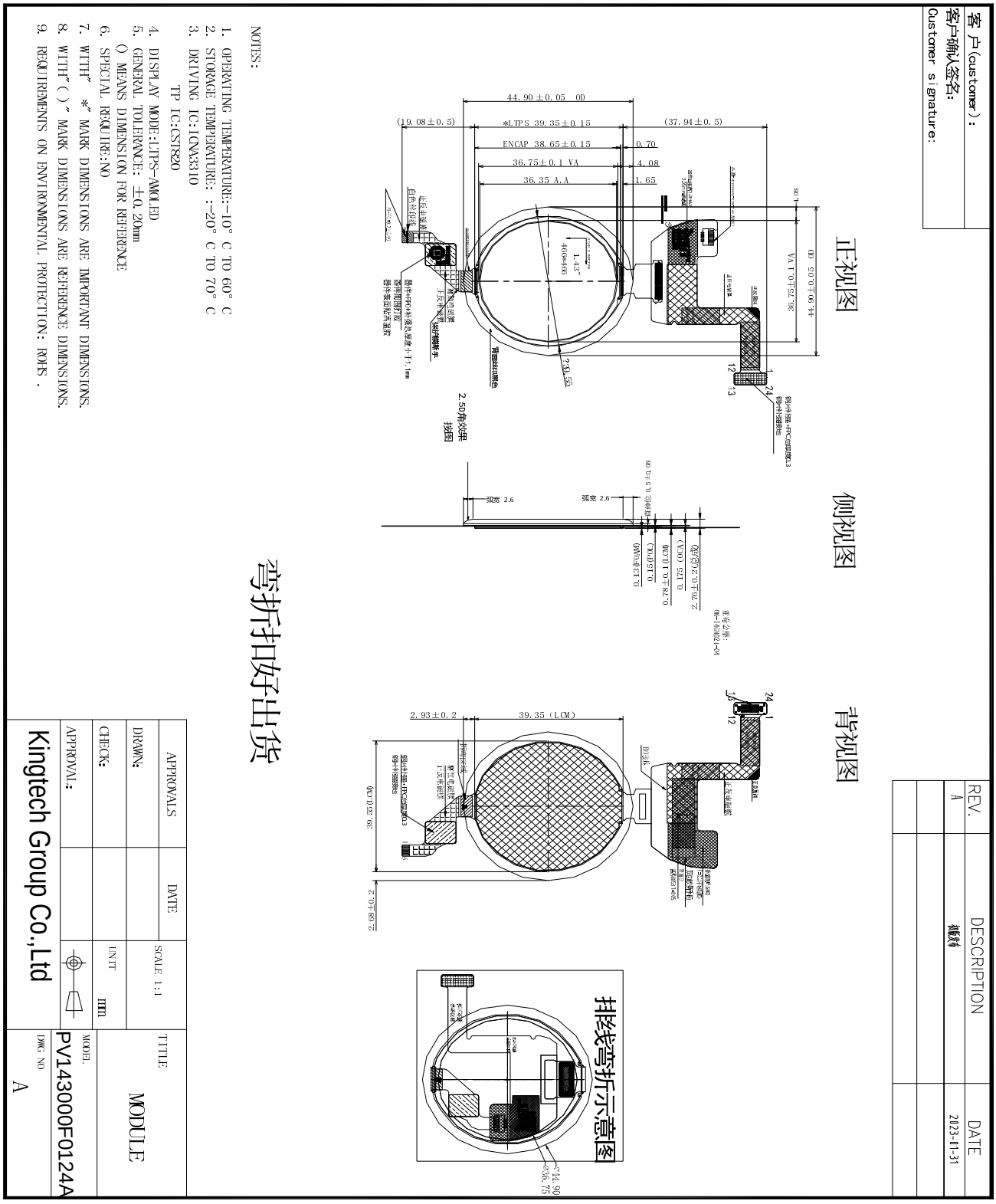
REVISION RECORD

Version	Revision Items	Page	Name	Date
1.0	First release			20230523

1.General Spec

Item	Standard values	Unit 单位
Diagonal Inch	1.43	inch
Dot arrangement	466(W) x RGB x 466(H)	dots
Pixel pitch	78 x 78	μm
Display mode	AMOLED	/
Driver IC	ICNA3310/3311	/
Module size	44.9(V) x 44.9(W) x 2.76(T)	mm
Active area	ϕ36.35	mm
Interface	QSPI	-
Operating temperature	-10~60	℃
Storage temperature	-20~70	℃

2.Mechanical drawing



3. Interface description

Pin No.	Symbol	Description
1	CS	Chip Select Signal in MIPI DBI Type-B(MPU) and Type-C(SPI) Active Low
2	D0	Serial Data Input in Quad-SPI
3	D1	Serial Data Input in Quad-SPI
4	SCL	Synchronous Clock Signal in MIPI DBI Type-B(MPU) and Type-C(SPI)
5	D3	Serial Data Input in Quad-SPI
6	D2	Serial Data Input in Quad-SPI
7	GND	Ground.
8	VCI_EN	Enable for POWER IC
9	RST	Device reset signal (0 : Enable ; 1: Disable)
10	MTP	External Voltage Input for OTP Data Program
11	NC	NC
12-13	GND	Ground.
14	TE	Tearing effect output pin to synchronize MCU to frame
15	VDD	Power Supply for Analog Circuits VCI < 0.05V (When power is turned off
16-17	VBAT	Analog Power Input for POWER IC Input Voltage Range: 3.4V to 5.5V
18	GND	Ground.
19	TPSCL	Touch Panel Clock
20	TPSDA	Touch Panel Data
21	TPRST	Touch Panel Reset
22	TPINT	Touch Panel interrupt
23	TPVDD	Touch Panel Power Supply
24	GND	Serial Data Input in Quad-SPI

4. Absolute Maximum Ratings

Item	Symbol	Min	Max	Unit
Supply voltage (Display)	VDD	-0.3	3.6	V
	IOVCC	-0.3	3.6	V
	VBAT	3.4	5.5	V
	VCI_EN	1.8/3.3		V
Operating temperature range	Top	-10	+60	℃
Storage temperature range	Tst	-20	+70	℃
Storage humidity	HD	-	90	%RH

5. DC Characteristics

DC Characteristics List

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit	Notes
Power generation & Operation Voltage							
AVDD booster voltage	AVDD	Operating Voltage	4.5	-	6.5	V	
VCL booster voltage	VCL	Operating Voltage	-5.0	-	-3.5	V	
Analog Operating voltage	VREFP	Operating Voltage	0.5	-	5.0	V	
Analog Operating voltage	VREFN	Operating Voltage	-5.0	-	-0.5	V	
Analog Operating voltage	I_ELVDD	Operating Voltage	2.0	-	5.0	V	
Analog Operating voltage	I_ELVSS	Operating Voltage	-5.4	-	-0.5	V	
Gamma reference voltage	VGMP	Operating Voltage	2	-	6.3	V	
Gamma reference voltage	VGSP	Operating Voltage	0	-	4.5	V	
VGH booster voltage	VGH	Operating Voltage	3		10.6	V	
VGL booster voltage	VGL	Operating Voltage	-15		-2	V	
Voltage difference between VGH and VGL	VGH-VGL	|VGH-VGL| ≤30			30	V	
I/O operating voltage	VDDI	I/O supply voltage	1.65	-	3.3	V	
LOGIC INPUT/ OUTPUT							
Logic High level input voltage	V_{IH}		0.8× VDDI	-	VDDI	V	1
Logic Low level input voltage	V_{IL}	-	VSS	-	0.2× VDDI	V	1
Logic High level output voltage	V_{OH}	I_{OH} = -0.1mA	0.8× VDDI	-	VDDI	V	2
Logic Low level output voltage	V_{OL}	IOL = +0.1mA	VSS	-	0.2× VDDI	V	2
Logic High level leakage	I_{LIH1}	Vin = 0 to *VDDI*	-	-	1	μA	1,2
Logic Low level leakage	I_{LIL1}	Vin = 0 to *VDDI*	-1	-	-	μA	1,2
Source OP Output							
Output deviation voltage	V_{dev}	Sout ≧4.2V Sout ≦0.8V			TBD	mV	4
Output deviation voltage	V_{dev}	4.2V>Sout>0.8V			TBD	mV	
Output offset voltage	V_{OFSET}				TBD	mv	
Stand-by Current							

6.Electron-optical Characteristics

5.1 Electrical Characteristics

5.1.1 Power Characteristic:

Item	Symbol	Min.	Typ.	Max.	Unit	Remark
AMOLED Power positive	ELVDD	3.25	3.3	3.35	V	-
AMOLED power Negative	ELVSS	-3.35	-3.3	-3.25	V	Ref
Digital Power supply	VDDIO	1.7	1.8	1.95	V	Ref
Analog Power supply	VCI	3.25	3.3	3.35	V	Ref

1) Normal Mode

Power Supply: IOVCC=1.8V VCI=3.3V ELVSS=-3.3V ELVDD=3.3V

Frame Frequency: F_{frame} =60HZ @ 25degC, Brightness 450 nits, Command Mode,

Display Condition	Symbol	Min.	Typ.	Max.	Unit	Remark
100% Pixel On 450nits	IELVDD /ELVSS	-	33	38	mA	Ref
	IVCI	-	6	7.2	mA	Ref
	IVDDIO	-	3	3.6	mA	Ref

2) Idle Mode

Power Supply: IOVCC=1.8V VCI=2.8V

Frame Frequency: F_{frame} =15HZ @ 25degC, Brightness:100nits, OPR:10%,Command Mode(driver ic fc power)

Display Condition	Symbol	Min.	Typ.	Max.	Unit	Remark
10% Pixel On 100 nits	IELVDD /ELVSS	-	-	-	mA	Supplied by Driver IC
	IVCI	-	5	6	mA	Ref
	IVDDIO	-	1.2	1.5	mA	Ref

3) Deep Standby Mode

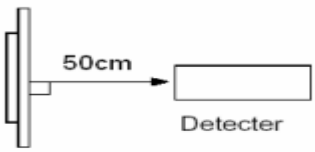
Display Condition	Symbol	Min.	Typ.	Max.	Unit	Remark
Deep Standby(Vci Off)	Power Consumption	-	-	<50	uW	Ref

Test condition: VDDIO=1.8V , Vbat=3.7V ,Ta=25℃

Item		Symbol	Condition	Value			Unit	Note
				Min	Typ	Max		
Luminance		Bp	θ=0°	400	450	--	cd/m2	Note 1
Uniformity		△Bp	Φ=0°	85		-	%	Note 2
Viewing Angle	Left	θ_L	Cr≥10	80	85	-	Deg.	Note 3
	Right	θ_R		80	85	-		
	Top	ψ_T		80	85	-		
	Bottom	ψ_B		80	85	-		
Contrast Ratio		CR	θ=0°	10000	100000	-	-	Note 4
Response Time		Tr+Tf	Φ=0°	-	2	3	ms	Note 5

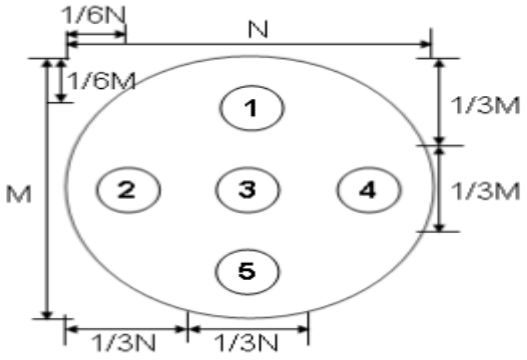
NTSC Ratio	NTSC	CIE1931		100	-	%	-
Flicker	-	-	-	-	-30	dB	-
Gamma	-	-	1.9	2.2	2.5		Note 6
Crosstalk	ΔCT	-	-	-	1.1		Note 7

- Measured value at the center point of panel must be after more than 5 minutes while backlight turning on.



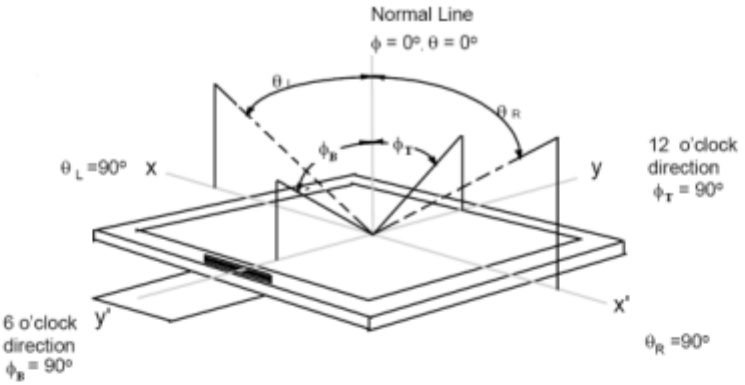
Note 2: Uniformity

- The test condition is at 25℃ and measured on the surface of display module.
- Measurement equipment: CS2000 or similar equipments.
- The luminance uniformity is calculated by using following formula:
- △ Bp = Bp (Min.) / Bp (Max.)×100 (%)
- Bp (Max.) = Maximum brightness in 5 measured spots
- Bp (Min.) = Minimum brightness in 5 measured spots.



Note 3: The definition of Viewing Angle

Refer to the graph below marked by ϑ and Φ

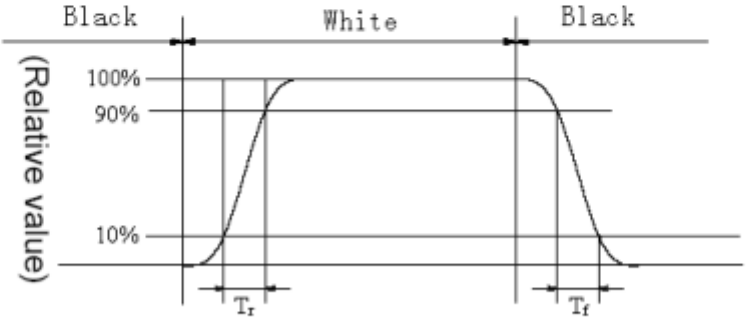


Note 4: **The definition of Contrast Ratio**:

$$\text{Contrast Ratio (CR)} = \frac{\text{Luminance When AMOLED is at "White" state}}{\text{Luminance When AMOLED is at "Black" state}}$$

Note 5: **Definition of Response time.**

The output signals of photo detector are measured when the input signals are changed from "black" to "white" (Voltage falling time) and from "white" to "black" (Voltage rising time), respectively. The response time is defined as the time interval between the 10% and 90% of amplitudes. Refer to figure as below.



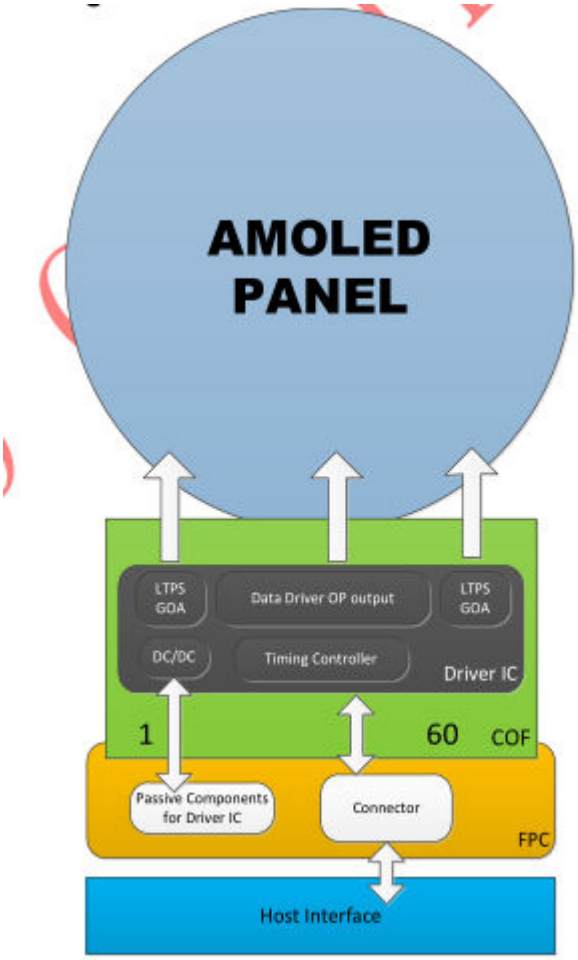
Note 6: Gamma curve

The whole curve's tolerance must control within +/-0.3, test the gray scale below:
8, 16, 25, 33, 41, 49, 58, 66, 74, 82, 90, 99, 107, 115, 123, 132, 140, 148, 156, 165, 173, 181, 189, 197,206, 214, 222, 230, 239, 255

Note 7: **Crosstalk**

There should be no visible cross-talk in normal direction of the display when the two

7. System Block Diagram



8. AC characteristic& Power On/Off Sequence

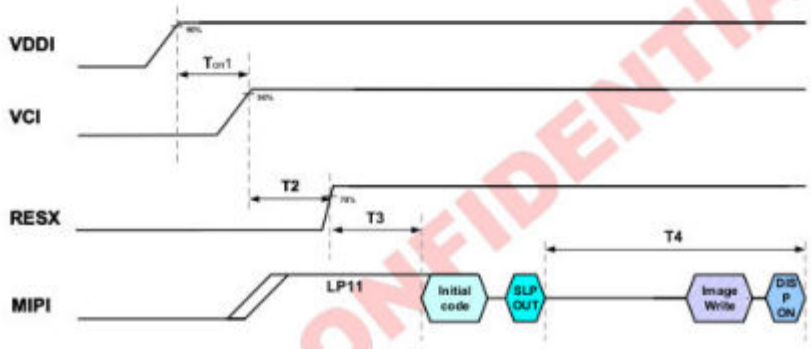
Power ON Sequence

The power on sequence for different power input modes are shown below figures.

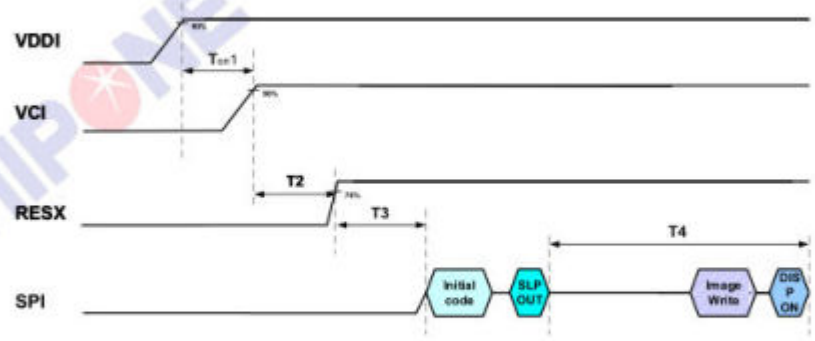
Power ON Sequence Timing

Symbol	Description	Value			Unit	Remark
		Min.	Typ.	Max.		
Ton1	VDDI on to VCI on delay	>0			us	
T2	VDDI on to valid to RESET high	10			ms	
T3	RESET high to first command	10			ms	
T4	Sleep-out command received to Display on command received.	60			ms	

The Power on sequence is shown as below.



MIPI Power ON Sequence



SPI Power ON Sequence

Note 1: *Unless otherwise specified, timings herein show cross point at 50% of signal/power level.*

Note 2: *This power-on sequence is based on adding Schottky diode on VGL pin to ground.*

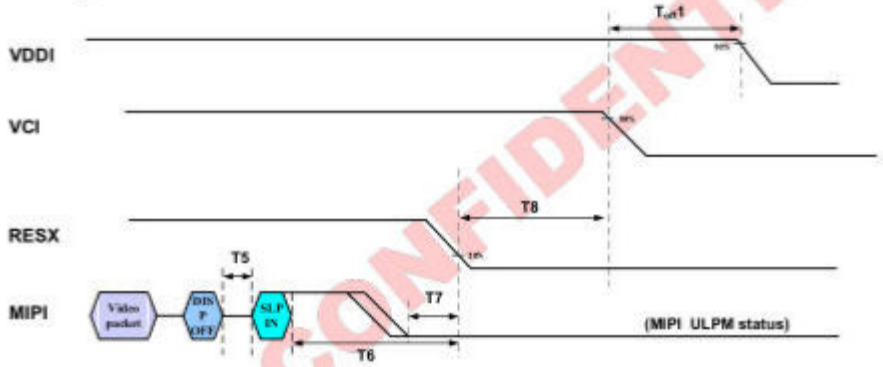
Power OFF Sequence

The power off sequence for different power input modes are shown below figures.

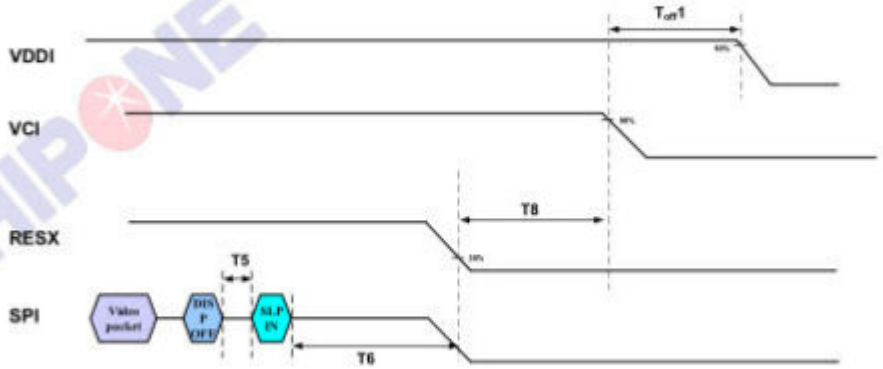
Power OFF Sequence Timing

Symbol	Description	Value			Unit	Remark
		Min.	Typ.	Max.		
Toff1	VCI off to VDDI off delay	>0			us	
T5	Display-off command received to Sleep-in command delay	>0			us	
T6	Sleep-in command received to valid to RESET low	83			ms	@60Hz
T7	MIPI ultra low power mode to valid to RESET low	0			us	
T8	RESET low to VCI off delay	0			us	

The power off sequence is shown as below:



MIPI Power off sequence



SPI Power off sequence

Note 1: *Unless otherwise specified, timings herein show cross point at 50% of signal/power level.*

Note 2: *Keep VGH is equal to or larger than VCI during power off sequence.*

Absolute Maximum Ratings

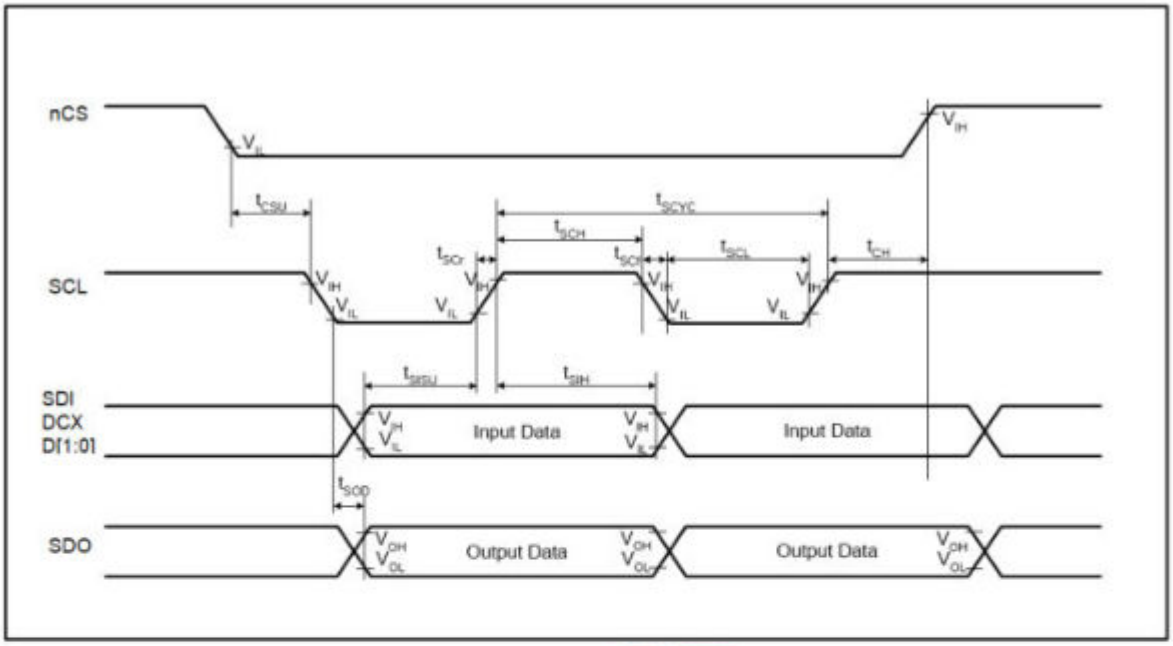
The absolute maximum rating is listed in below table. It may lead permanently damaged when the ICNA3311 is used out of the absolute maximum rating.

To use the ICNA3311 within the following electrical characteristics limit is strongly recommended for normal operation. If these electrical characteristic conditions are exceeded during normal operation, the ICNA3311 will malfunction and be poor reliability.

Absolute Maximum Ratings List

Item	Symbol	Rating			Unit
		Min.	Typ.	Max.	
Power supply voltage	VDDI ~ VSSD	-0.3	-	+5.5	V
Power supply voltage	VCI (VCIA, VCIC, VCIR) ~ VSSA	-0.3	-	+5.5	V
Supply voltage	AVDD ~ VSSA	-0.3	-	+6.6	V
Supply voltage	AVSS ~ VCL	-0.3	-	+5.0	V
Supply voltage	VGH ~ VGL	|VGH-VGL| ≦30			V
Operating temperature	Topr	-40		+85	℃
Storage temperature	Tstg	-55		+125	℃
Input voltage	Vin	-0.3		VDDI+0.3	V

Serial Interface Characteristics (QUAD SPI)



Parameter	Symbol	Conditions	Specification			Unit	Notes
			MIN	TYP	MAX		
SCL	T_{SCYC}	Clock cycle (Write)	20	-	-	ns	
	T_{SCYC}	Clock cycle (Read)	100		-	ns	
	T_{SCH}	Clock "H" pulse width (Write)	6.5	-	-	ns	
	T_{SCH}	Clock "H" pulse width (Read)	45	-	-	ns	
	T_{SCL}	Clock "L" pulse width (Write)	6.5	-	-	ns	
	T_{SCL}	Clock "L" pulse width (Read)	45	-	-	ns	
	T_{SCr}	Clock rise time	-	-	3.5	ns	
	T_{SCf}	Clock fall time	-	-	3.5	ns	
CSX	T_{CSU}	Chip select setup time	10	-	-	ns	
	T_{CH}	Chip select hold time	10	-	-	ns	
SDI DCX D[1:0]	T_{SISU}	Data input setup time	4	-	-	ns	
	T_{SIH}	Data input hold time	4	-	-	ns	
SDO	T_{SOD}	Data output setup time	-	-	45	ns	
	T_{SOH}	Data output hold time	5	-	-	ns	

***Note 1**: Logic high and low levels are specified as 20% and 80% of VDDI for Input signals.*

***Note 2**: Ta = -30 to 85 °C, VDDI=1.65V to 3.3V, VCI=2.7V to 3.6V, GND=0V*

***Note 3**: The max SCL sequence of 4-wire QSPI transferring RGB888, RGB666 and RGB555 is 50Mhz.*

9. QUAD SPI Interface/MIPI DC Characteristics

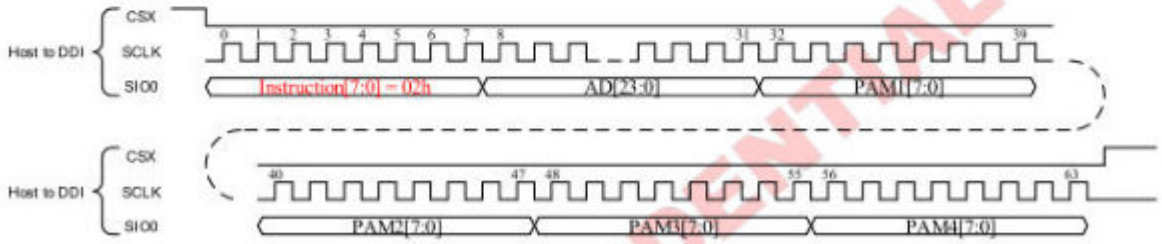
Write Cycle and Sequence

The QUAD SPI interface write command sequences are described in the following figure as below.

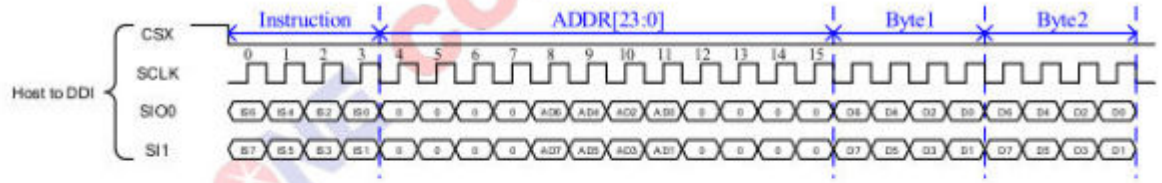
QSPI write protocol contain as below :

Instruction[7:0] = 02h	Command write
AD[23:0] = {8'h00, CMD[7:0], 8'h00}	Driver IC command address
PAM[7:0]	Driver IC parameters

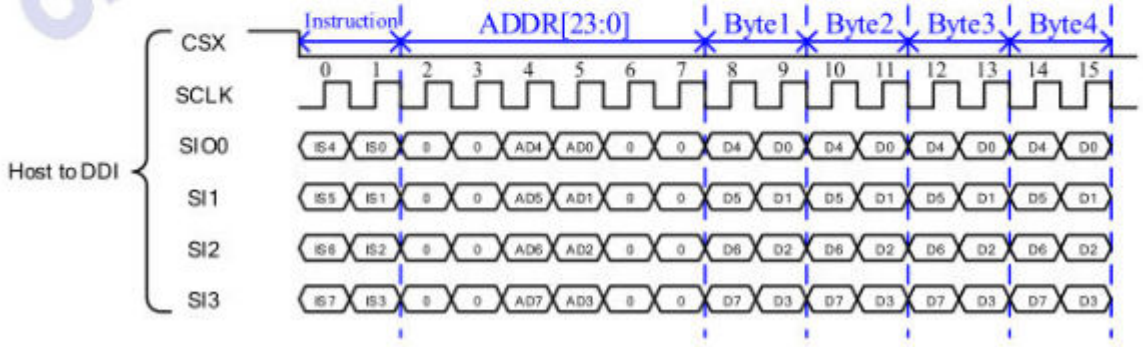
QSPI 1-wire write



QSPI 2-wire write

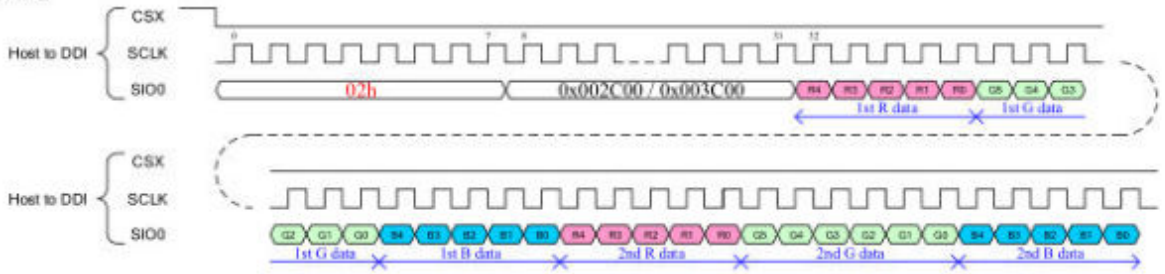


QSPI 4-wire write

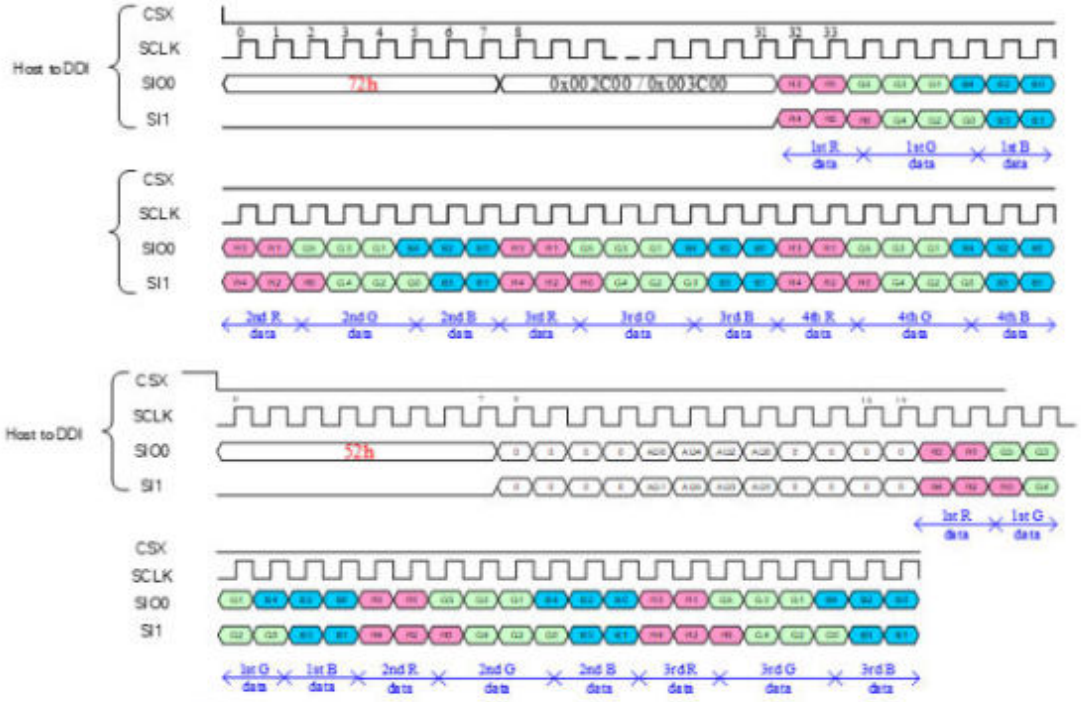


RGB565:

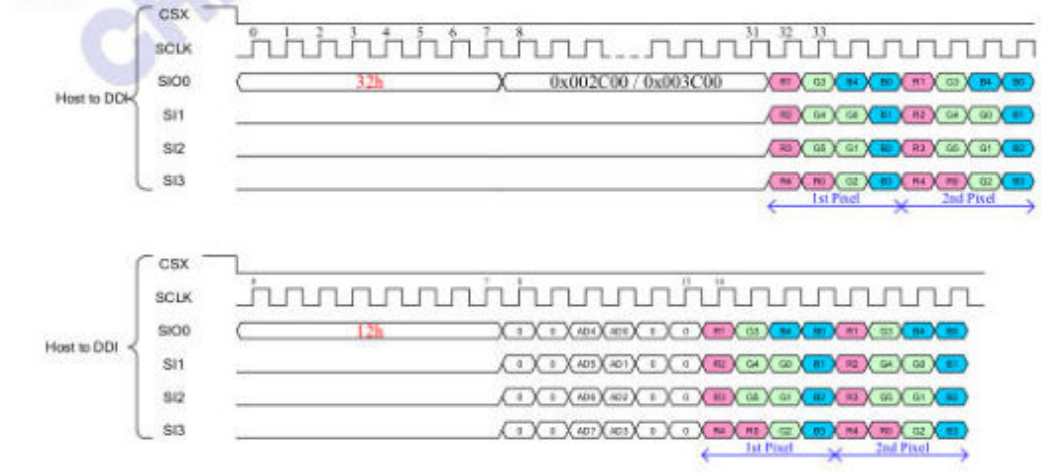
1-wire



2-wire



4-wire



MIPI DC Characteristics

DC Characteristics for DSI LP Mode

Condition : Ta =25℃,VDDI =1.65V~3.3V, VCI =2.7V~3.6V,

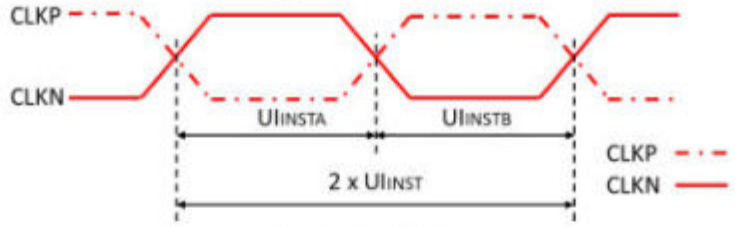
DC Characteristics List for DSI LP Mode

Parameter	Symbol	Conditions	Specification			Unit	Notes
			MIN	TYP	MAX		
Logic high level input voltage	V_{IHLPCD}	LP-CD	450		1350	mV	
Logic Low level input voltage	V_{ILLPCD}	LP-CD	0		200	mV	
Logic high level input voltage	V_{IHLPRX}	LP-RX (CLK,D0)	880		1350	mV	
Logic Low level input voltage	V_{ILLPRX}	LP-RX (CLK,D0)	0		550	mV	
Logic Low level input voltage	$V_{ILLPRXULP}$	LP-RX(CLK ULP mode)	0		300	mV	
Logic high level input voltage	V_{OHLPTX}	LP-TX(D0)	1.1		1.3	V	
Logic Low level input voltage	V_{OLLPTX}	LP-TX(D0)	-50		50	mV	
Logic high level input voltage	I_{IH}	LP-RX,Vin =0~1.3V			10	μA	
Logic Low level input voltage	I_{IL}	LP-RX,Vin =0~1.3V	-10			μA	
Input pulse rejection	SGD	DSI-CLKP/N,DSI-DnP/N			300	Vps	1

Note 1: Peak interference amplitude max. 200mV and interference frequency min. 450MHz.

Spike/Glitch Rejection

High Speed Mode - Clock Timings



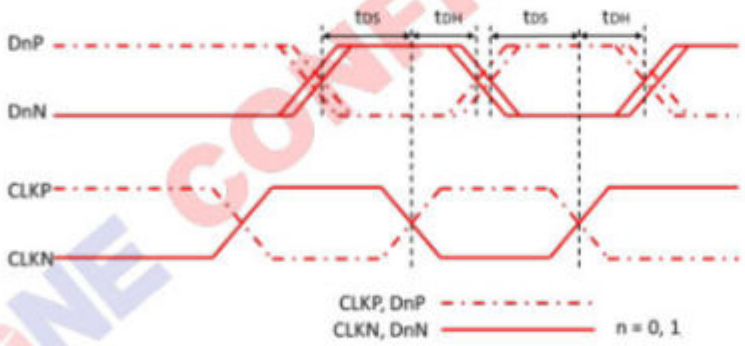
Clock Timing

High Speed Mode - Clock Timing

Signal	Symbol	Parameter	Specification			Unit	Notes
			MIN	TYP	MAX		
CLK P/N	2xUIINST	Double UI instantaneous	4		25	nS	
CLK P/N	UIINSTA, UIINSTB	UI instantaneous Half	2		12.5	nS	1

Note 1: *UI = UIINSTA = UIINSTB.*

High Speed Mode - Clock / Data Timings



DSI Clock / Data Timings

High Speed Mode - Clock / Data Timing

Signal	Symbol	Parameter	Specification			Unit	Notes
			MIN	TYP	MAX		
Dn P/N	tDS	Data to Clock Setup time	0.15*UI			UI	
(n=0, and1)	tDH	Clock to Data Hold time	0.15*UI			UI	

High Speed Mode - Rising and Falling Timings

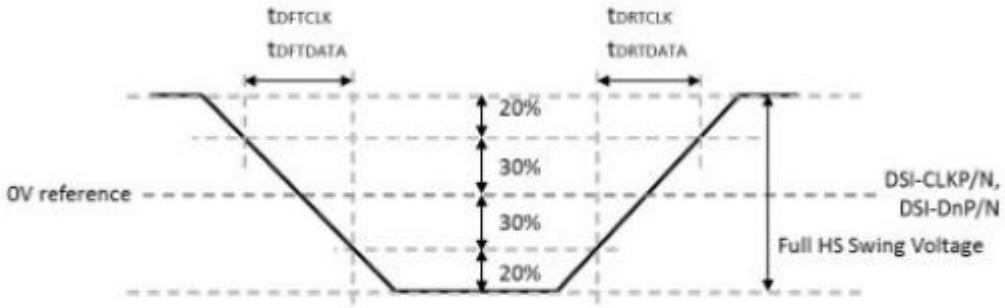


Figure 6-2 Rising and Falling Timings

High Speed Mode - Rising and Falling Timing

Parameter	Symbol	Conditions	Specification			Unit	Notes
			MIN	TYP	MAX		
Differential Rise Time for Clock	t_{DRTCLK}	CLKP/N	150pS		0.3*UI		2,3
Differential Rise Time for Data	$t_{DRTDATA}$	DnP/N	150pS		0.3*UI		1,2,3
Differential Fall Time for Clock	t_{DFTCLK}	CLKP/N	150pS		0.3*UI		2,3
Differential Fall Time for Data	$t_{DFTDATA}$	DnP/N	150pS		0.3*UI		1,2,3

Note 1: *DnP/N, n =0, and 1.*

Note 2: *The display module has to meet timing requirements, which are defined for the transmitter (MCU) on MIPI D-PHY standard.*

Note 3: *DSI-CLK+ = CLKP.*
DSI-CLK- =CLKN.
DSI-D0+ =D0P.
DSI-D0- =D0N.

DC Characteristics for DSI HS Mode

Condition : Ta =25℃,VDDI =1.65V~3.3V, VCI =2.7V~3.6V.

DC Characteristics List for DSI HS Mode

Parameter	Symbol	Conditions	Specification			Unit	Notes
			MIN	TYP	MAX		
Input voltage common mode range	V_{CMCLK} V_{CMDATA}	CLKP/N, DnP/N	70		330	mV	1,2
Input voltage common mode variation (≦450MHz)	$V_{CMRCLKL}$ $V_{CMRDATAL}$	CLKP/N, DnP/N	-50		50	mV	3
Input voltage common mode variation (≧450MHz)	$V_{CMRCLKM}$ $V_{CMRDATAM}$	CLKP/N, DnP/N			100	mV	
Low-level differential input voltage threshold	V_{THLCLK} $V_{THLDATA}$	CLKP/N, DnP/N	-70			mV	
High-level differential input voltage threshold	V_{THHCLK} $V_{THHDATA}$	CLKP/N, DnP/N			70	mV	
Single-ended input low voltage	V_{ILHS}	CLKP/N, DnP/N	-40			mV	2
Single-ended input high voltage	V_{IHHS}	CLKP/N, DnP/N			460	mV	2
Differential input termination resistor	R_{TERM}	CLKP/N, DnP/N	80	100	125	Ω	
Single-ended threshold voltage for termination enable	V_{TERM_EN}	CLKP/N, DnP/N			450	mV	
Termination capacitor	C_{TERM}	CLKP/N, DnP/N			14	pF	

Note 1: Includes 50mV (-50mV to 50mV) ground difference.

Note 2: Without VCMRCLKM / VCMRDATAM .

Note3: Without 50mV (-50mV to 50mV) ground difference.

Note4: Dn =D0,and D1.

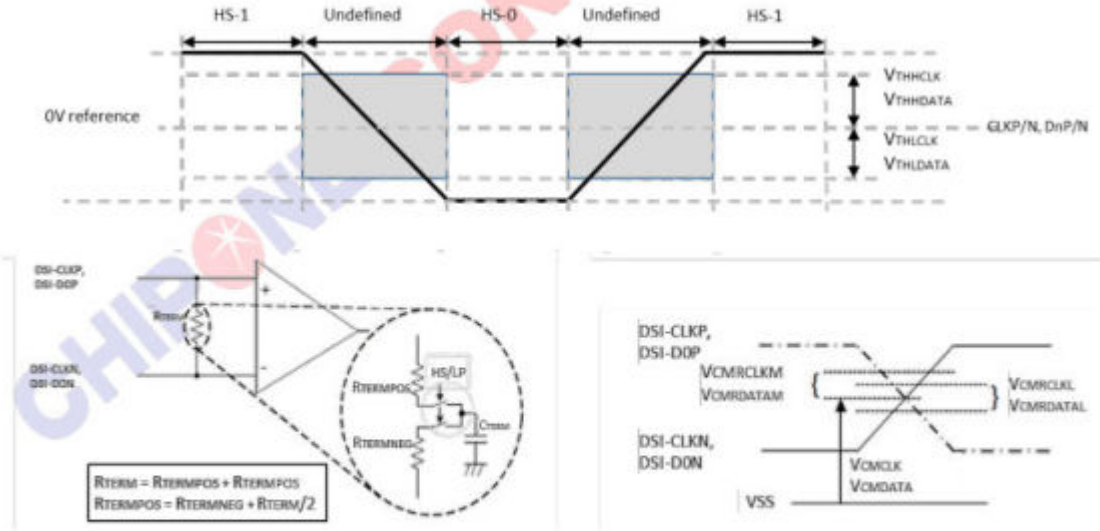


Figure 6-1 Differential voltage range, termination resistor and Common mode voltage

10.Reliability test conditions and methods

No	Test Item	Test condition	Criterion
1	High Temperature Storage	70℃±3℃ 48H Power off	Inspection after 4 hours storage at room temperature,the sample shall be free from defects: 1. Air bubble in the LCD; 2.Seal leak; 3.Non-display; 4.missing segments; 5.Glass crack; 6.Current Idd is twice higher than initial value. 7.The surface shall be free from damage. 8.The electric characteristic requirements shall be satisfied
2	Low Temperature Storage	-20℃±3℃ 48H Power off	
3	High Temperature Operation	60℃±3℃ 48H Power on	
4	Low Temperature Operation	-10℃±3℃ 48H Power on	
5	High Temperature & Humidity Operation	60℃±3℃ 90%RH 48H Power off	
6	Temperature Cycle	-20℃←→25℃←→70℃ 30min 5min 30min 5 cycle Power off	